Parallel Connection of Silicon Carbide MOSFETs for Multichip Power Modules

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Abstract

SiC technology has been under a rapid growth in the last decades, thanks to its wide band gap material superiorities, which leads to a higher breakdown voltage, a higher temperature limitation, a smaller thermal impedance and a faster switching speed of the SiC power devices compared to Si. Among the several kinds of SiC power devices, SiC MOSFET is considered to be the most promising to be commercialized and an alternative of Si IGBT, because of its unipolar device structure, voltage gate control and normally-off transistor property.

Along with the benefits of SiC MOSFETs, there are also some challenges from the manufacture and application points of view. The less mature manufacture process limits the yield and the single die size of the SiC MOSFETs, which results a smaller current capability of a single SiC MOSFET die. Consequently, in high current application, the paralleled connections of SiC MOSFET dies are required. In addition, the fast switching speed makes SiC MOSFETs more sensitive to the circuit parasitic parameters. The circuit parameters in the present Si IGBT power module packaging technology may be too critical for SiC MOSFETs.

This dissertation investigates the switching characterization of SiC MOSFETs regarding the influence of switching loop stray inductance and common source stray inductance. The pulse current measurement methods of fast switching speed power devices are summarized and a new method witch silicon steel current transformer is presented.

With the knowledge of the switching characterization of SiC MOSFETs, the paralleled connection of SiC MOSFETs is studied regarding both the influence of device mismatch and circuit mismatch. The circuit mismatches of switching loop stray inductance and common source stray inductance are first analyzed and experimentally investigated.

Then the DBC layout of a power module with paralleled SiC MOSFETs is presented and mathematically analyzed considering the influence of the circuit mismatch among the paralleled dies. It is revealed that there is a large common source stray inductance mismatch among the paralleled SiC MOSFETs, which leads to a significant transient current imbalance during

the switching period. Besides the circuit mismatch, a current coupling effect is also found in the DBC layout, which aggravates the transient current imbalance among the paralleled SiC MOSFET dies. The discussions about the effects of the auxiliary source connections for the paralleled dies are presented and the source of the transient current imbalance is concluded.

To mitigate the transient current imbalance in the traditional DBC layout, a novel DBC layout with split output is proposed. First, the working mechanism of the split output topology is studied, which turns out to be able to improve the efficiency compared to the traditional half bridge. Besides the split output topology benefits, compared to the traditional DBC layout, the proposed DBC layout significantly reduces the circuit mismatch and current coupling effect, which consequently improves the current sharing performance among the paralleled SiC MOSFET dies in the power module. The proposed DBC layout is not only limited for SiC MOSFETs, but also for Si IGBTs and other voltage controlled devices.

The main contribution of this dissertation is that it mathematically and experimentally investigates the influence of the circuit mismatch on the paralleled connection of SiC MOSFETs. It reveals the circuit mismatch and the current imbalance in the traditional DBC layout of power modules with paralleled dies. Based on that, a novel DBC layout for current imbalance mitigation is proposed. The more important point is that it starts the study of the DBC layout regarding the current distribution among the paralleled dies in the power module. The analysis method of the DBC layout provides new design guidelines and evaluation criteria of the DBC layout for multichip power modules with paralleled power semiconductor dies.

Danske Abstrakt

Gennem de sidste årtier er der sket en stor udvikling i SiC teknologien. Dette skyldes en række overlegne materiale egenskaber ved havledermaterialer med et stort bånd gab såsom høj gennemslagsspænding, større temperaturtolerance, bedre varmeledning samt evnen til at operere ved høje skiftefrekvenser indenfor effektelektronik. Blandt de mange typer af SiC effektelektronik komponenter, virker SiC MOSFET komponenter som det mest lovende alternativ relativt til Si IGBT komponenter i forhold til kommercialisering, på grund af deres unipolære virkningsmåde, den gode kontrol over gate-spænding samt "normally" off egenskaberne ved denne transistor type.

Sammen med de nævnte fordele kommer dog også en række udfordringer udfra et produktions og anvendelses perspektiv. Fremstillingsprocessen for SiC er knap så moden og dette sætter begrænsninger på størrelsen af SiC MOSFET komponenterne med en mindre strømydelse for de enkelte komponenter til følge. Dette betyder igen at der skal anvendes flere komponenter i parallel i anvendelsesområder der kræver store strømstyrker. Derudover kan de hurtige reponstider for SiC MOSFET komponenter gøre at kredsløb med disse komponenter bliver mere følsomme overfor parasitiske kredsløbs elementer. Det kan dermed vise sig at de parasitiske elementer der er den IGBT baseret teknologi ikke er tilstrækkeligt små til at kunne implementere SIC MOSFET komponenter direkte.

I denne afhandling undersøges skifteegenskaberne ved SiC MOSFETS og hvordan typiske strø-induktanser påvirker disse egenskaber. I afhandlingen beskrives forskellige metoder til at lave målinger af strømpulser og en ny metode til at måle strøm i dobbelt puls test ved at anvende siliciumstål præsenteres.

Med afsæt i de undersøgte skifteegenskaber af SiC mosfet komponenterne undersøges eksperimentelt dernæst kredsløb med flere komponenter sat i parallel med særligt fokus på at analysere indvirkningen af forkert parring mellem komponenter og misforhold i kredsløbsdesign.

Herefter præsenteres et forslag til et DBC layout med paralleliserede SiC MOSFET komponenter som analyseres i forhold til kredsløbsmisforhold

mellem de indsatte komponenter. Arbejdet afslører at der et stort misforhold i "common mode" strø induktans mellem komponenterne, hvilket giver anledning til et stor transient misforhold i strømfordelingen under skiftecyklussen. Derudover påvises en strømkoblingseffekt i DBC layoutet der yderligere forværrer det transiente misforhold i strømfordelingen mellem SiC komponenterne. Betydningen af de ekstra forbindelser til "source" terminalen diskuteres efterfølgende og kilden til de transiente misforhold i strømfordelingen identificeres.

Som en løsning på ubalancen i strømfordelingen præsenteres efterfølgende et DBC layout der baserer sig på "Split Output" topologien. Virkningsprincippet i denne topologi præsenteres og det vises at dette kan forbedre effektiviteten set i forhold til en traditionel halv-bro topologi. Det demonstreres yderligere at det fremsatte DBC layout også reducerer problemerne forbundet med strøm misforholdene og strømkobling markant, hvilket følgelig forbedrer strømfordelingen mellem komponenterne –et resultat der ikke kun begrænser sig til SiC komponeneterne.

Afhandlingens primære videnskabelige bidrag er eksperimentelle såvel som matematiske undersøgelse af betydningen af kredsløbs misforhold i forhold til paralleliseringen af SiC MOSFET komponenter. Den afslører misforhold i kredsløbene og strømfordelingen I traditionelle DBC layouts og giver et bud på nyt kredsløb der imødekommer disse problemer. Undersøgelsen pointerer vigtigheden af at inddrage analyser af strømfordelingen mellem paralleliserede komponenter i forbindelse med DBC layout og bidrager dermed med nye retninglsinjer og kvalitetskriterier i forbindelse med optimeringen af DBC kredsløb til mange-komponent effekt moduler hvor halvleder komponeneter skal paralleliseres.

Contents

Publication list:

Chapter 2:

1. H. Li, S. Munk-Nielsen, 'Challenges in switching SiC MOSFET without Ringing', *PCIM Europe* 2014, Germany.
2. H. Li, S. Munk-Nielsen, 'Detail study of SiC MOSFET switching characteristics', *PEDG* 2014, Ireland.
3. H. Li, S. Beczkowski, S. Munk-Nielsen, K. Lu, Q. Wu, 'Current measurement method for characterization of fast switching power semiconductors with silicon steel current transformer', *APEC* 2015, USA.

Chapter 3:

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Chapter 5:

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List of abbreviations and symbols

MOSFET	metal-oxide-semiconductor field-effect transistor
IGBT	insulated-gate bipolar transistor
JFET	junction field effect transistor
SiC	silicon carbide
GaN	gallium nitride
Si	silicon
DBC	direct bonded copper
PCB	printed circuit board
ESR	equivalent series resistance
R_{on}	on state resistance
V_{th}	threshold voltage
I_D	MOSFET drain current
I_{di}	diode forward current
U_{DC}	DC link voltage
L_g	gate loop stray inductance
L_s	common source stray inductance
L_d	switching loop stray inductance
u_{GS}	gate source voltage
u_{DS}	drain source voltage

1 Introduction

1.1 Background

Power semiconductors are widely used in the application areas of consumer goods (e.g. washing machines), industry (e.g. pumps and wind power) and transportation [1]. In low power application areas, single discrete semiconductor devices are capable of transferring the energy. In high power application, power modules with paralleled dies are usually needed. Typical applications of power modules with paralleled dies are in wind power [2] and traction systems [3, 4]. In wind power systems, the power converters are often using 1700V/1400A transistor/diode power modules. The power modules are built with a number of paralleled Silicon (Si) Insulated Gate Bipolar Transistors (IGBT) and diode devices. The rating of a single IGBT die is about 100-200A. In the traction systems, the power modules cover a large range of voltages (1700V-6500V) and currents (600A-2400A) [3].

Power semiconductors with Si technology have been the main work horse of power electronics for the last more than two decades. Among all power device structures, the Metal-Oxide-Semiconductor (MOS) controlled unipolar devices are preferable due to the feasible voltage control and the low device switching losses. In the voltage range below 600V, Si Metal-Oxide-Semiconductor-Field-Effect-Transistors (MOSFETs) are the favorable power devices. However, the on-resistance (R_{on}) of the MOSFET increases as a function of the blocking voltage more than its square [5]. With a higher blocking voltage, the R_{on} is too high that the conduction loss of the MOSFET takes most of the power. In the voltage range above 600V, especially higher than 1000V, the Insulated Gate Bipolar Transistor (IGBT), which improves the conducting properties by the injection of additional carriers, becomes the main power device. The side effect of the injected charge carriers is the ‘tail current’, which increases the turn off losses and limits the switching speed of IGBT. Another power device with the improved MOS structure is the super junction MOSFET [6]. The proposed CoolMOS with super junction structure successfully reduces R_{on} and pushes the MOSFET blocking voltage up to 600V-1000V [5, 7]. In the voltage range above 1000V, at present, the Si IGBTs are still the dominant switches.

With the development of power electronics, the requirements to the power semiconductors continuously increase: fast switching speed, high switching frequency, high efficiency, high reliability, high power density and high operation temperature [8-10]. The manufactures have been continuously improving the device performance. From the IGBT point of view, the structure design trade-off between the Saturation Voltage of Collector-Emitter ($V_{CE(sat)}$) and the switching losses has been optimized [4] since the invention of Si IGBT [11, 12]. The power density of the IGBT increased 3 times from the first generation to the 4th generation [13]. The potential of the Si material has been utilized close to the physical limit of Si material. At this moment, Wide Band Gap (WBG) materials, e.g. Silicon Carbide (SiC) and Gallium Nitride (GaN), draw the attention of power electronics due to their material superiorities.

1.2 SiC technology

SiC technology has been under a rapid growth in the last decade to meet the increasing demand of power semiconductors. Compared to the Si material, SiC possesses a higher band gap, a higher thermal conductivity, and a higher saturated electron drift velocity [14].The properties comparison between SiC and Si is illustrated in Table.1 [14, 15].

Table1. SiC and Si property comparison

Property	Si	4H-SiC
Bandgap, E_g (eV)	1.12	3.26
Critical Electric Field, E_c(V/cm)	2.5×10^5	2.2×10^6
Thermal Conductivity, λ (W/cm•K)	1.5	4.9
Saturated electron drift velocity, v_{sat} (cm/s)	1×10^7	2×10^7

SiC material has a 3 times higher bandgap of Si. It makes SiC be able to stand much higher temperature operation and more radiation. Even at 600 ℃, the intrinsic concentration is not the limitation, but rather the metal contacts and the packaging [16]. The labeled temperature limitation 150 ℃ of the commercial SiC power devices is mostly limited by the package technology [17-19].

The critical electric field of SiC is almost 10 times of Si. The high critical breakdown field allows a much higher doping concentration and thinner drift

layer at the same breakdown voltage level. Consequently, the specific on resistance for the drift region in 4H-SiC is about 2000 times smaller [14] than the Si counterpart at the same breakdown voltage, as shown in Figure.1.1 [20].

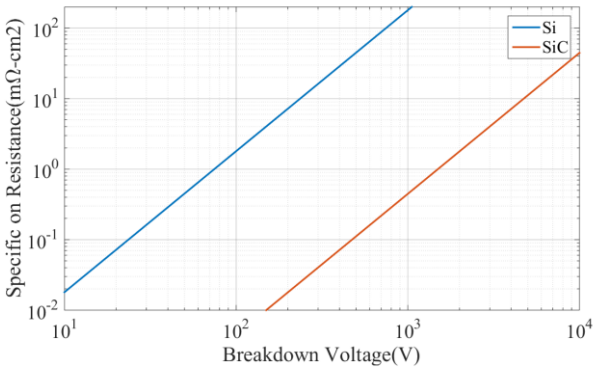


Figure 1.1 Specific on-resistance in drift regions in Si and 4H-SiC

SiC material has a more than 3 times higher thermal conductivity than Si. The high thermal conductivity leads to a lower thermal resistance from junction to case. It means that the SiC power devices can dissipate more power with the same temperature rise. The power density, therefore, can be improved.

The saturated electron drift velocity determines the switching speed capability of the power devices. The SiC material has a twice saturated electron drift velocity than Si. Therefore, the SiC power devices are expected to switch much faster than Si power devices[14].

1.3 Silicon Carbide MOSFETs

Among all the SiC power devices, SiC MOSFET is the most promising device to be an alternative of Si IGBT, which has been the dominating power switches in high voltage range in the last two decades.

On the one hand, the material superiorities make the SiC MOSFET capable of handling breakdown voltage as high as Si IGBT (1.2kV, 1.7kV, 3.3kV, 4.5kV and 6.5kV) or even higher. In the voltage range above 1kV, the commercial SiC MOSFETs rated at 1.2kV [21] and 1.7kV are available [22]. 3.3kV SiC MOSFETs are also reported in some laboratory research works

[23, 24]. In the medium voltage range, Cree has released the 10kV SiC MOSFETs and there are some research works on it [25-27]. The 10kV SiC MOSFETs are comparable to the 6.5kV Si IGBTs [28, 29]. Above 10kV, SiC IGBTs are under development [30, 31]. On the other hand, compared with Si IGBT, the unipolar structure of SiC MOSFET and the SiC material properties results reduced switching losses and fast switching speed [32, 33]. Consequently, the power electronic converters built with SiC MOSFET can operate at a higher switching frequency and lower switching losses [33]. The higher switching frequency leads to a smaller size of the passive components while the reduced power losses allow a smaller cooling system. The passive components and the cooling system usually take the main volume of the total power electronic system. The decreased volume of the passive filter and the cooling system reduce the cost and improve the power density on the system level [8].

Compared with the other SiC unipolar device, e.g. the Junction Field Effect Transistor (JFET), SiC MOSFET enjoys a voltage gate control and a normally-off transistor property, which makes SiC MOSFET more controllable, more reliable and more attractive to the industrial applications.

However, despite the favorable properties of SiC MOSFETs, there are also some challenges for their manufacture and application. One challenge is that the SiC technology is not as mature as the Si technology. A number of material and fabrication issues still need to be addressed, including the stability of the threshold voltage [34], the reliability of the body diode [35] and the gate oxide [36]. In the fabrication process, SiC has a higher level of defects, compared with Si [37]. The defects near the interface oxide layer may act as electron traps and cause fixed charges, which lead to shifts in the threshold voltage of the device in long time operation [19]. In the extreme case, the SiC MOSFET may become a normally-on device because of the threshold voltage shifting.

The less mature manufacture process also limits the yields and the single die size of SiC MOSFETs. Consequently, at present, the SiC MOSFET single die current capability is not as large as Si IGBT. In high current applications, parallel connection of SiC MOSFETs is needed [38-40]. Another unfavorable property of SiC MOSFETs is the intrinsic body diode. The

forward voltage drop of the intrinsic body diode is relatively high [41]. And there is still reverse recovery current because of the intrinsic body diode [18]. In a bridge configuration, the body diode reverse recovery effect may lead to extra switching losses [42, 43]. Furthermore, the utilization of the body diode may affect the reliability of the SiC MOSFETs. Due to the unfavorable properties of the intrinsic body diode, the manufactures usually recommend using an external paralleled SiC schottky diode [41], which has no reverse recovery current and relative low forward voltage drop.

From the application point of view, the fast switching speed of SiC MOSFETs, i.e. high d*i*/dt and d*v*/dt, can be a double-edged sword. It is true that the fast switching speed can reduce the switching losses, thereby increasing the switching frequency and achieving some merits on the system level. However, due to the fast switching speed, SiC MOSFETs are more sensitive to the circuit parasitic parameters. The physical circuits lead to stray inductance by bond wires, Print Circuit Board (PCB) or Direct Bonded Copper (DBC) traces, bus-bar and the connectors [44]. With Si IGBT and the low switching speed, the stray inductance may not be too critical. However, for SiC MOSFETs and high d*i*/dt, the same insertion stray inductance may cause a significant voltage drop or overshoot [44], which may cause the SiC MOSFET operate beyond the Safe Operation Area (SOA) of the devices. The parasitic parameters of the present packaging technology for Si devices may be too high for the SiC devices. From this point of view, the present packaging technology not only limits the temperature ceiling but also affects the switching performance of the SiC MOSFETs. Therefore, more advanced packaging technology or improvement based on the current technology is required to fully utilize the potential of the SiC MOSFETs.

At present, the price of SiC devices is still higher than comparable Si devices. But the system cost with the SiC MOSFETs can be lower than the counterpart with Si IGBT. Moreover, the price of SiC device has dramatically decreased in the recent five years, as shown in Figure 1.2 [33].

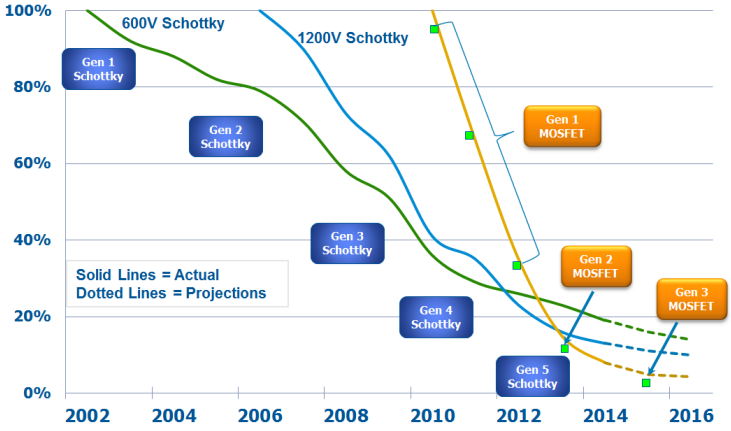


Figure 1.2 SiC cost reductions from volume and device refinement. Green line is for 600V SiC schottky diode. Blue line is for 1200V SiC schottky diode. Orange line is for 1200V SiC MOSFETs [33].

1.4 Parallel connection of power semiconductors

In high current and high power applications, parallel connection with discrete packaged devices and power modules [45, 46] with paralleled semiconductor dies are usually employed. For the parallel connection of power semiconductors, an important design issue is the current distribution and thermal uniformity among the paralleled devices. A non-uniform current distribution may lead to thermal inequality and result a low ruggedness [47, 48] of the power module and the converter. Moreover, it causes de-rating and lowers the electrical properties of the power module [49].

Parallel connection of power semiconductors, e.g. MOSFETs and IGBTs, is not a new topic. Parallel connection of Si MOSFETs was discussed in 1981 by J.B. Forsythe [45]. The causes of the current non-uniform distribution were attributed to device parameters mismatch, power circuit parameters mismatch and gate driver circuit mismatch. Besides this research work, there were some similar discussions about the parallel connection of Si MOSFETs from the power semiconductor manufactures. However, they mainly focused on the influence of the device parameters mismatch while the circuit parameters mismatch was not fully understood. For the parallel connection of Si IGBTs [50, 51], the discussion is similar to that with Si MOSFETs. The

difference is that the influence devices parameters of IGBT are the $V_{CE(sat)}$ and V_{th} while for Si MOSFET counterparts are R_{on} and V_{th}.

For the influence of the circuit parameters mismatch, Kun Xing, Fred C. Lee etc. [48] found that the bond wires parasitcs affect the current sharing between the paralleled IGBT chips and between the bond wires. The non-uniform current distribution can lead to wire bond's fatigue and power module failure. A. Consoli etc. [52] described the effects of the internal layout on the performance of IGBT power modules. Takeshi Ohi etc. [49] investigated the influences of the bus bar structure on the current imbalance in an IGBT module. Both A. Consoli and Takeshi Ohi presented the transient current imbalance among the paralleled IGBT dies and attributed the imbalance to the parasitic parameters, e.g. the inductance caused by the bond wires and the bus bars. However, the conclusion is still just talking about making symmetric layout design. The estimations do not figure out the most critical parameters for the current distribution and there are no guidelines of how to make a symmetric layout design. Therefore, with the limited area of the DBC pattern, the optimized design has not been achieved with the present knowledge.

Parallel connection with SiC devices, including SiC JFETs [53, 54] and SiC MOSFETs [55], has also been studied since the SiC devices were available. However, the emphasis is still on the evaluation of the device parameters mismatch. Yang Xue, Fred Wang etc. [56] proposed an active current balancing method for paralleling SiC MOSFETs. But it is only suitable for parallel connection of the discrete package devices and the parallel quantity is also limited to two. Regarding the power modules with paralleling SiC devices, numerous papers make great efforts on the high temperature operation of the SiC MOSFET power modules [38, 39, 57]. Even some researchers also paid attention to the DBC layout design for power modules with paralleled dies [58-60], the power module is always considered as a whole cell and the optimization is reducing the total switching loop stray inductance. The parasitic parameters influences on the current sharing among the paralleled SiC dies are always overlooked in the published research works.

1.5 Research motivations and objective

From the previous discussion of the background, it is aware that more efforts are needed before the superiorities of the SiC MOSFETs can be fully utilized, especially in the power modules with paralleled dies.

First, the switching characteristics of the SiC MOSFETs are not fully investigated. One reason is that the fast switching speed of SiC MOSFETs requests a higher bandwidth of the measurement method, especially for the current measurement. There is a need to pay attention to the current measurement otherwise the following switching losses calculation and the thermal system design will be based on an inaccurate precondition. Moreover, the influences of the circuit parasitic parameters on the switching behavior of the SiC MOSFETs are not discussed either. Therefore, a research work on the switching performance related to the parasitic parameters and based on an accurate current measurement can help better understand the switching characteristics of SiC MOSFETs.

In high current applications, the parallel connection of the SiC MOSFETs is a challenge. For the parallel connection of power devices, the significant design issue is the current imbalance among the paralleled power devices, both for discrete devices and the bare dies in power modules. The aim of this project is to figure out the current distribution in the SiC MOSFETs power module with the state-of-the-art packaging technology and successively find the most critical parameters for the current sharing performance. The final target is to give the knowledge of the DBC layout design for power module with paralleled dies. With the DBC layout design knowledge, a better current sharing performance in the SiC MOSFET power module should be achieved and thereby improve the electrical properties and the reliability of the power modules.

1.6 Thesis outline

To address the above issues and better utilize the advantages of SiC MOSFETs, especially in power modules with paralleled dies, this dissertation is organized as below.

Chapter 1 is the introduction part, including the application background of power semiconductors, the SiC material and SiC MOSFET superiorities, the challenges for the application of SiC MOSFETs, the challenges for the

parallel connection of semiconductors in power modules and finally the objective of this thesis.

Chapter 2 gives the switching characterization of the SiC MOSFETs. To get the switching behavior of the SiC MOSFETs, the current measurement methods (e.g. Rogowski Coil, Pearson Current Monitor and Coaxial Current Shunt) for fast switching power devices are first compared. Based on the existing current measurement method, a two stage current measurement method with silicon steel current transformer is first presented. With the accurate current measurement, the switching behavior of the SiC MOSFETs is presented regarding the stray inductance, including the switching loop stray inductance and the common source stray inductance. The current and voltage oscillations during the switching transient are mathematically analyzed. Challenges of switching the SiC MOSFETs without severe ringing are discussed. A thorough understanding of SiC MOSFET switching characteristics is summarized.

Chapter 3 investigates the parallel connection of the SiC MOSFETs. The influences of the circuit mismatch on the parallel connection of SiC MOSFETs are first presented. First, the device parameters variations regarding R_{on} and V_{th} are obtained. With a clear scope of the device mismatch, the R_{on} and V_{th} mismatch influence on the current sharing performance is studied. The circuit mismatch influence study is based on the conclusion of Chapter 2. A circuit mismatch influence with respect to the switching loop stray inductance as well as the common source stray inductance is first investigated. Both the device mismatch and circuit mismatch study is done with discrete SiC MOSFETs.

Chapter 4 starts the research works about the parallel connection in the power modules layout. With the knowledge from Chapter 3, the DBC layout of a power module with paralleled SiC MOSFET dies is first discussed regarding the circuit mismatch. The DBC layout of the power module is modeled including the stay inductance of the DBC traces and the bond wires. Common source stray inductance mismatch, which has a large influence on the transient current sharing performance among the paralleled dies, is investigated in the DBC layout. Furthermore, it reveals that there is a current coupling effect in the DBC layout of the power module. The current

coupling effect further aggravates the current imbalance. With the knowledge got from the specific DBC layout, the DBC layout with auxiliary source bond wires is also studied. With the mathematic modeling and analysis, it is found that auxiliary source bond wires in the power module works in a different way from the Kelvin-Source connection. The merits and drawbacks with the auxiliary source bond wires are discussed regarding the current distribution in the power module. With the discussion of these two DBC layouts, the essence of the circuit mismatch in the DBC layout of the power module is summarized, which clearly explain the current imbalance among the paralleled dies in the power module.

In Chapter 5, the analysis and experimental study of a split output half bridge topology is presented. The split output half bridge aims to decouple the intrinsic body diode and the output capacitance of the SiC MOSFETs. The current commutation mechanism is first analyzed. LTspice simulation and experimental results help to analyze the working mechanism of the split output topology. The efficiency comparison between the normal half bridge and the half bridge with split output is presented with the switching frequency from 10kHz to 100kHz. It shows that the split output is suitable for high switching frequency operation. With the understanding of the split output, a novel DBC layout with split output is proposed to mitigate the circuit mismatch in the traditional DBC layout of the power module with paralleled dies. Mathematic analysis is presented with the comparison to the traditional DBC layouts. Simulation and experimental results shows that the proposed DBC layout has a smaller circuit mismatch. Moreover, the current coupling effect is also reduced and thereby the current sharing performance is improved. The proposed DBC layout can be used both for the normal half bridge and the half bridge with split output.

Finally, Chapter 6 gives the conclusion and the future work plan. The contributions of this dissertation are as the following. The switching characterization under the influence of parasitic parameters is investigated. The existed pulse current measurement methods are compared and a new method with silicon steel current transformer is proposed. The current sharing performance of paralleled SiC MOSFETs is studied under the influence of circuit and device mismatches. The present DBC layout is

revealed to have large circuit mismatch which lead to transient current imbalance. A novel DBC layout design is proposed which has reduced circuit mismatch. With the proposed DBC layout, the transient current imbalance is dramatically mitigated. The present packaging technology for Si IGBT may not be suitable for SiC MOSFET. For fully utilizing the fast switching speed capability of SiC MOSFET, new packaging technology is expected.

2 Switching characterization of SiC MOSFETs

Switching characterization of the power semiconductors is a key for the switching losses calculation, heatsink design and life time prediction of the power converters. In the design process of the power converter, the bus-bar design should refer to the current switching speed, i.e. d*i*/dt, of the power semiconductors. The thermal system design relies on the power losses, including conduction loss and switching losses, of the power semiconductors. Switching losses are determined by the time integration of the current and the voltage product during the switching transient. In a bridge configuration, the dead-time duration is also decided by the switching speed of the power semiconductors.

SiC MOSFETs switching characterization has not been fully investigated on the circuit level from the presented literatures, especially under the influence of the parasitic parameters with the present package technology. This chapter exploits the switching performance of the SiC MOSFET, including the current measurement method comparison, switching oscillation mechanism and switching characterization with parasitic inductance.

2.1 Switching oscillation mechanism

2.1.1 Ideal switching characterization

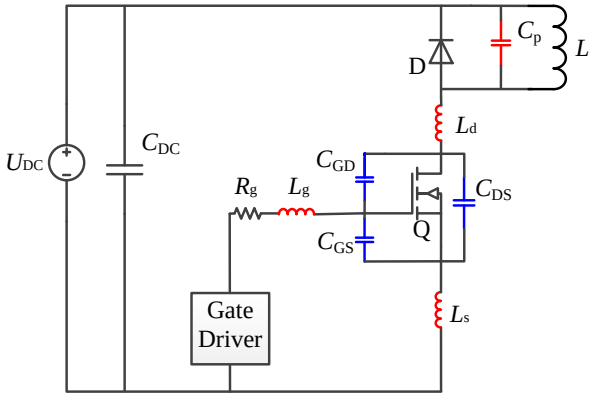


Figure 2.1 Double pulse test circuit

The switching characterization of the SiC MOSFET is investigated with a double pulse test circuit, as shown in Figure 2.1.

u_{DC} is the DC link voltage. C_{DC} is the DC link capacitance. R_g is the external gate resistance. L is the inductance of the load inductor. D is the freewheeling diode and Q is the SiC MOSFET. The red color components are the circuit parasitic parameters. C_p presents the sum capacitance of the diode junction capacitance and the equivalent paralleled capacitance of the load inductor. L_g is the gate loop stray inductance. L_d is the total switching loop stray inductance, including the equivalent series inductance of the DC link capacitor, the stray inductance of the connection from the DC link capacitor to the MOSFET and the package parasitic inductance in the switching loop. L_s is called common source stray inductance, which is the stray inductance both in the power current switching loop and the gate current switching loop. The blue color components are the parasitic capacitance of the MOSFET. C_{DS}, C_{GS} and C_{GD} are respectively the parasitic drain source, gate source and gate drain capacitance of the MOSFET.

Without the circuit parasitic parameters, an ideal switching behavior of the MOSFET is described as in Figure 2.2. During turn-on process, u_{GS} first increase at the moment of t_0. Before u_{GS} increases above V_{th}, the MOSFET does not turn on and the drain current I_D keeps zero. From t_1, u_{GS} starts to be larger than V_{th}, the MOSFET turns on and I_D increases until it reaches the magnitude of the load current, at the time of t_2. From t_2, the drain source voltage u_{DS} begins to drop and u_{GS} keeps stable until t_3, at which moment u_{DS} decrease to 0. From t_3 to t_4, u_{GS} increases and the channel resistance of the MOSFET decreases, thereby the MOSFET has a minimum conduction loss. The turn-off process is a reverse procedure of the turn-on.

A simulation switching characterization is presented in Figure 2.3. The LTpice double pulse test circuit is with the SiC MOSFET (C2M0160120D) bare die spice model provided from Cree and an ideal diode with no capacitive charge. With an ideal diode, it is convenient to adjust the capacitive charge from the load inductor and the diode. U_{DC}=600V and the on-state drain current is set to be 20A. The u_{GS} is set to be -5V for turn-off and 20V for turn-on. The simulation switching characterization without the circuit parameters matches with the ideal switch characterization.

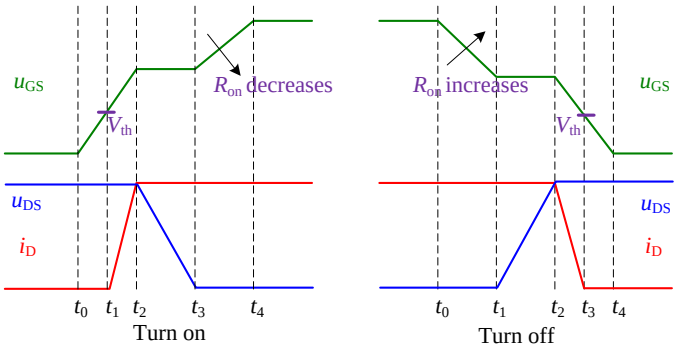


Figure 2.2 Ideal switching characterizations of MOSFET

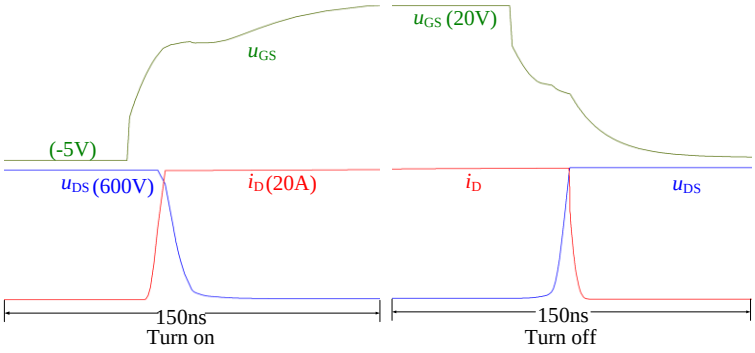


Figure 2.3 Simulation results without the circuit parasitic parameters

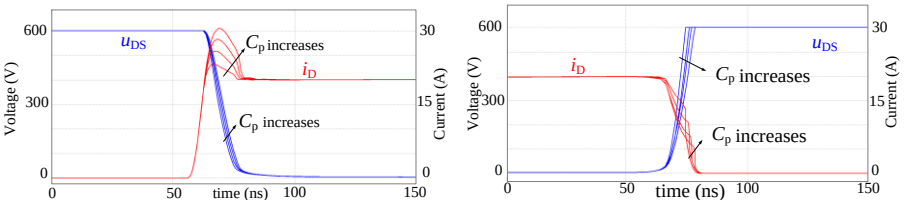
2.1.2 Switching characterization with circuit parasitic parameters

The influence of the parasitic parameters on the switching behavior of the SiC MOSFET is individually explored. It means that when one parasitic parameter influence is studied, the other parasitic parameters are set to zero.

C_p has a significant influence on the turn-on drain current. In Figure 2.1, before the MOSFET turns on, the diode conducts the load current and the voltage drop on C_p is almost zero. During turn on transient, the load current commutates from the diode to the MOSFET. u_{DS} decreases from u_{DC} to $U_{DS(on)}=I_D \times R_{on}$ while the voltage on C_p increases simultaneously from zero to u_{DC}. Therefore, during the turn-on transient, there is a current for charging C_p and after turn on this current should drop to zero, as shown in (2.1). During turn-on, this current, consequently, leads to a current overshoot of i_D. The i_D overshoot magnitude depends on the capacitance of C_p and the switching

speed of u_{DS}. A simulation switching behavior with different C_p values (50pF, 100pF, 150pF and 200pF) are shown in Figure 2.4. The overshoot of i_D increases with the increases of the C_p capacitance. On the other hand, C_p affects the switching speed u_{DS}. With a higher C_p, the voltage switching speed decreases due to the capacitor has a tendency of keeping the voltage.

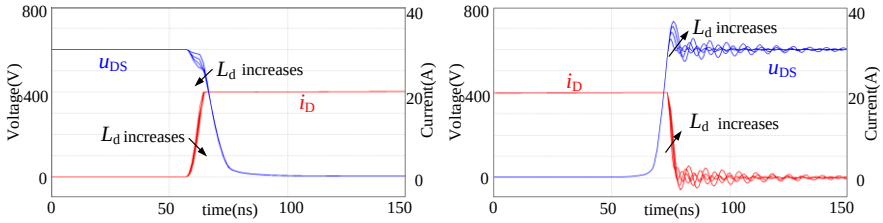
$$i_{Cp} = C_p \frac{du_{Cp}}{dt} = -C_p \frac{du_{DS}}{dt} \tag{2.1}$$



(a) (b)

Figure 2.4 Switching behavior with different C_p (50, 100, 150, 200pF) (R_g=20Ω) (a) turn on (b) turn off

L_d affects the u_{DS} switching behavior, as explained in (2.2). During turn-on, i_D increases and therefore u_{DS} has a voltage dip before the drain current reaches stable. During turn-off, i_D decreases and thereby u_{DS} has an overshoot. The amplitude of the u_{DS} dip and overshoot depends on the inductance of L_d and the current switching speed. The simulation results with different L_d are shown in Figure 2.5. Besides the effects on the u_{DS}, L_d can also cause the oscillations on the drain current after turn-off, as seen in Figure 2.5. This oscillation is formed by L_d and the junction capacitance of the MOSFET.



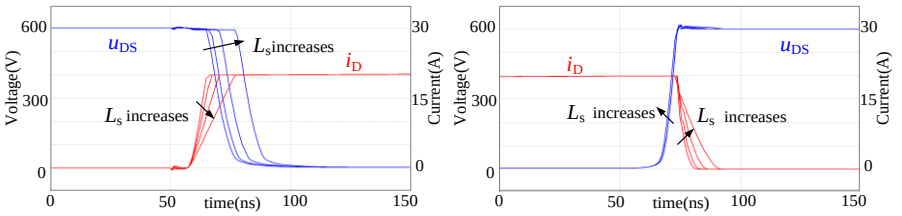
(a) (b)

Figure 2.5 Switching behavior with different L_d (5nH 10nH 15nH 20nH) (R_g=20Ω) (a) turn on (b) turn off

$$u_{DS}=u_{DC}-L_d\frac{di_{Ld}}{dt}=u_{DC}-L_d\frac{di_D}{dt} \tag{2.2}$$

In the saturation region during the switching transient, the MOSFET drain current is determined by u_{GS}. L_s is the common source stray inductance. Therefore it influences the switching behavior by its feedback effect on the gate source voltage u_{GS}, as in (2.3). During turn-on, i_D increases and L_s causes a negative voltage added to u_{GS}. Consequently, the turn-on speed decreases. While during turn-off, i_D decreases and L_s leads to a positive voltage added to u_{GS}. As results, the turn-off speed also decreases. In summary, L_s slows down the switching speed of the MOSFET. The simulation results with different L_s are shown in Figure 2.6. L_s slow down the turn-on speed of u_{DS} but it does not affect the u_{DS} turn-off behavior. That is because the L_s affect the u_{GS} by the drain current. During turn-off, u_{DS} first increases before the falling down of i_D. Consequently, L_s has a larger influence on the turn-on process than on the turn-off process. The turn-on loss is affected by L_s.

$$u_{GS}=U_{driver}-i_gR_g-L_s\frac{di_S}{dt}\approx U_{driver}-i_gR_g-L_s\frac{di_D}{dt} \tag{2.3}$$



(a) (b)

Figure 2.6 Switching behavior with different L_s (1nH 2nH 4nH 8nH) (R_g=20Ω) (a) turn on (b) turn off

L_g has the similar effect with the L_s. The difference is that L_g only see the gate current and it does not conduct the power current, as seen in (2.4). Compared to i_D, i_g is much smaller. Therefore, the switching behavior has a much lower sensitivity to the L_g inductance. The simulation results with different L_g are shown in Figure 2.7. To see the effect of L_g, the gate resistance is set to 5Ω to get a higher switching speed.

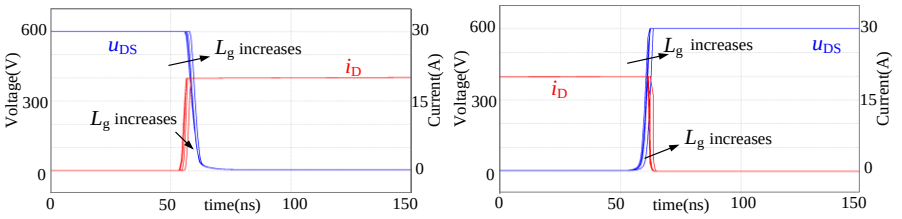


Figure 2.7 Switching behavior with different L_g (5nH 10nH 20nH 40nH) (R_g=5Ω) (a) turn on (b) turn off

$$u_{GS} = U_{driver} - i_g R_g - L_g \frac{di_g}{dt} \tag{2.4}$$

The effect of R_g is also investigated. The simulation results are as in Figure 2.8. With the increase of R_g, the switching speed decreases and the switching losses increase. The switching losses can be estimated with the cross area of u_{DS} and i_D.

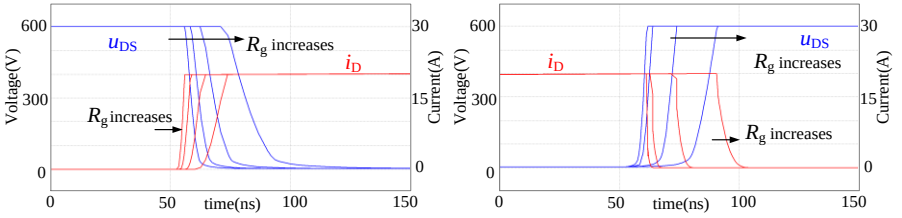


Figure 2.8 Switching behavior with different R_g (5 Ω 10 Ω 20 Ω 40Ω) (a) turn on (b) turn off

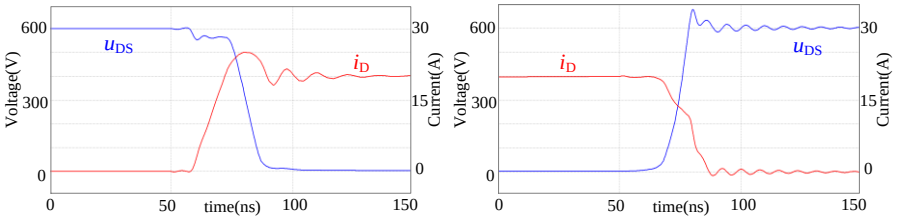
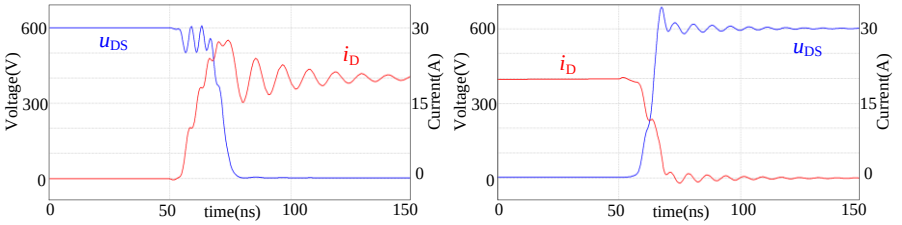


Figure 2.9 Switching behavior with R_g=20Ω L_g=5nH L_s=5nH L_d=20nH C_p=100pF (a) turn on (b) turn off

Figure 2.9 shows the switching behavior with the parasitic parameters. With the same parasitic parameters, if the gate resistance decreases from 20Ω to 5Ω, the switching behavior is as Figure 2.10. With a higher switching speed, the drain current and drain source voltage has more oscillations. The turn-on oscillation is formed by L_d and C_p while the turn-off oscillation is caused by L_d and C_{DS}. With the higher switching speed, the SiC MOSFET has a higher sensitivity to the parasitic parameters than the Si IGBT.



(a) (b)

Figure 2.10 Switching behavior with R_g=5Ω L_g=5nH L_s=5nH L_d=20nH C_p=100pF (a) turn on (b) turn off

2.2 Current measurement methods

An accurate voltage and current measurement method is the basis of investigating the switching behavior of the fast switching power semiconductors. Voltage measurement is relatively more feasible compared with the current measurement, especially for fast switching pulse current. An ideal pulse current measurement method for the fast switching power semiconductor characterization should possess the three essential qualities: the high bandwidth, the galvanic isolation and the feasible mechanical size. The -3dB high frequency bandwidth (BW) of the current sensor and the rise time (t_r) of the measured signal have a relation as in (2.5). If an accurate measurement is required, a 3 to 5 times BW margin should be guaranteed. For example, for a turn-on current with 20ns rise time, the corresponding -3dB high frequency bandwidth is 17.5MHz. Take a 5 times margin, the current sensor should have a high frequency bandwidth not lower than 87.5MHz.

$$BW = \frac{0.35}{t_r} \tag{2.5}$$

2.2.1 Current measurement methods comparison

At present, there are three pulse current measurement methods which are widely used in the area of power semiconductor switching characterization. They are Rogowski coil, Pearson current monitor, and coaxial current shunt, as shown in Figure 2.11.

Figure 2.11 Existing current measurement methods

The commercial Rogowski coil has a small tight loop with very thin wire. Moreover, the Rogowski coil has the galvanic isolation. Therefore, the insertion of the current measurement with Rogowski coil is very feasible. For the switching characterization of the fast switching device, the limitation of the commercial Rogowski coil is the relatively low bandwidth. The highest bandwidth of the commercial Rogowski coil is around 30MHz. Moreover, the measurement accuracy depends on the measurement position. The central position measurement is usually more accurate than the other positions in the coil loop.

The Pearson current monitor also has the galvanic isolation and the bandwidth of the Pearson current monitor can be up to 200MHz. But the Pearson current monitor has a large physical size and the insertion of the current monitor can lead to extra stray inductance, which affects the switching behavior of the power devices.

The coaxial current shunt has the highest bandwidth up to Giga Hertz. But the coaxial current shunt does not provide galvanic isolation. The coaxial current shunt is a precise resistor, which has to be inserted into the current loop. The insertion can also lead to extra stray inductance.

The three current measurement methods, Rogowski coil CWT03, Pearson 2877 and coaxial current shunt SDN-414-025, are compared with a double pulse circuit. The bandwidth of the three current measurement methods is

20MHz, 200MHz and 1200MHz, respectively. The current measurement comparison experimental results are shown in Figure 2.12.

With Figure 2.12, the Rogowski coil measurement has large turn-on current overshoot and extra oscillations during switching transient. The Pearson 2877 and coaxial current shunt SDN-414-025 have the similar measurement performance. The Pearson 2877 shows around 3ns measurement delay, which can be calibrated and compensated. A summary of the three current measurement methods is concluded in Table 2.1, regarding the high frequency bandwidth, the galvanic isolation and the mechanical size.

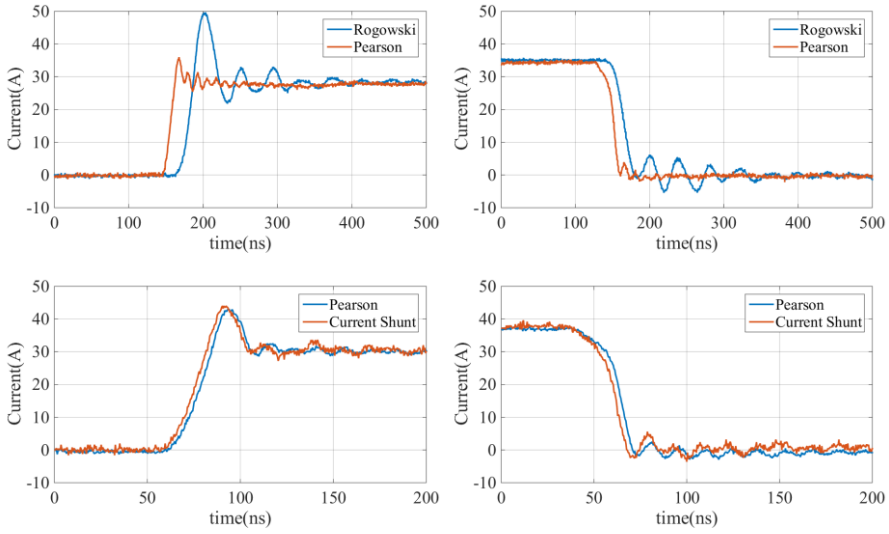


Figure 2.12 Comparison of Rogowski coil, Pearson and coaxial current shunt

Table 2.1 Performance evaluation of the current measurement methods for DPT application

	bandwidth	galvanic isolation	mechanical size
Rogowski coil	–	+	++
Pearson current monitor	+	+	–
Coaxial current shunt	++	–	+

Notes: + means good performance and – means bad performance

2.2.2 Current measurement with silicon steel current transformer

To avoid the drawback of the large mechanical size of the Pearson current monitor, a two stage current measurement method with Pearson 2878 is presented [61]. The two stage current measurement method has a first stage with a ferrite core current transformer, which is placed close to the transistor while the Pearson current monitor can be placed at a distance. The ferrite core transformer avoids the limitation of the mechanical size of the Pearson 2878. To evaluate the effect of the insertion of the ferrite core current transformer, an experiment comparison is shown in Figure 2.13. It shows that the ferrite core current transformer has little effect on the current measurement.

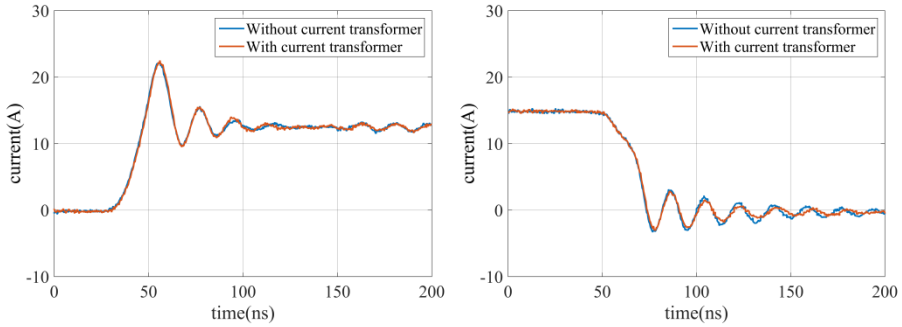


Figure 2.13 Experiment comparison of with and without the ferrite core current transformer

The two stage current measurement method, which is with the first stage ferrite core current transformer and the second stage Pearson current monitor, shows good performance regarding the high frequency bandwidth and the mechanical size. However, the ferrite core cannot be adjusted arbitrarily. Inspired by the ferrite core current transformer, a Silicon Steel Current Transformer (SSCT), which can be used in the two stage current transformer, is employed. Compared to the ferrite core, the SSCT has feasible mechanical design, which further widens the application area of the Pearson current monitor. The current transformer working mechanism for pulse current measurement is analyzed below.

The current transformer equivalent circuit is shown in Figure 2.14. i_1 is the current to be measured and i_2 is the measured current in the second winding by the Pearson current monitor. R_2 is the equivalent series resistance of the

second winding. L_1, L_2 and M are the inductance of first winding, the inductance of second winding and the mutual inductance, respectively. The relation of i_1 and i_2 is as (2.6), since the second winding is short circuit. During the switching transient, i_1 could be described as (2.7). According to (2.6), i_2 is calculated as (2.8), where $\tau_2=L_2/R_2$. In (2.10), σ is inductance leakage coefficient and N_2 is number of the second winding turns. The first winding has 1 turn. With (2.8) and (2.9), i_2 could be rephrased as (2.10) with the Taylor-series. According to (2.8), if t is quite small (during switching transient of fast switching power semiconductors), the relation of i_1 and i_2 is as (2.11), which indicates that the current transformer could express the change of i_1 during switching transient in a nearly linear way. However, if t is not short enough, the measured current i_2 could not linearly present i_1. The measurement error ξ is as (2.12). The analysis shows that current transformer is suitable for measuring switching transient current, especially fast switching transient current.

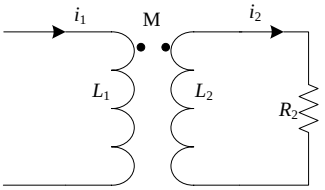


Figure 2.14 Current transformer equivalent circuit

$$R_2 i_2 + L_2 \frac{\mathrm{d}i_2}{\mathrm{d}t} + M \frac{\mathrm{d}i_1}{\mathrm{d}t} = 0 \tag{2.6}$$

$$i_1 = i_1(0) + kt \tag{2.7}$$

$$i_2 - i_2(0) = (-\frac{Mk}{R_2} - i_2(0))(1 - \mathrm{e}^{-\frac{t}{\tau_2}}) \tag{2.8}$$

$$\frac{M}{L_2} = \frac{1}{N_2}(1-\sigma) \tag{2.9}$$

$$i_2 - i_2(0) = -\frac{k}{N_2}(1-\sigma)(t - \frac{1}{2}\frac{t^2}{\tau_2} + \frac{1}{6}\frac{t^3}{\tau_2^2} + ...) \tag{2.10}$$

$$\frac{\mathrm{d}i_2}{\mathrm{d}t} \approx -\frac{1}{N_2}(1-\sigma)\frac{\mathrm{d}i_1}{\mathrm{d}t} \tag{2.11}$$

$$\xi = -\frac{k}{N_2}(1-\sigma)\left(\frac{1}{2}\frac{t^2}{\tau_2} - \frac{1}{6}\frac{t^3}{\tau_2^2} + \ldots\right) \tag{2.12}$$

The SSCT is experimentally studied both for characterization of the discrete packaged SiC MOSFET and the high current power module with Si IGBT. The two stage current measurement with SSCT is shown in Figure 2.15. Figure 2.16 shows the hardware prototype for the evaluation of the SSCTs.

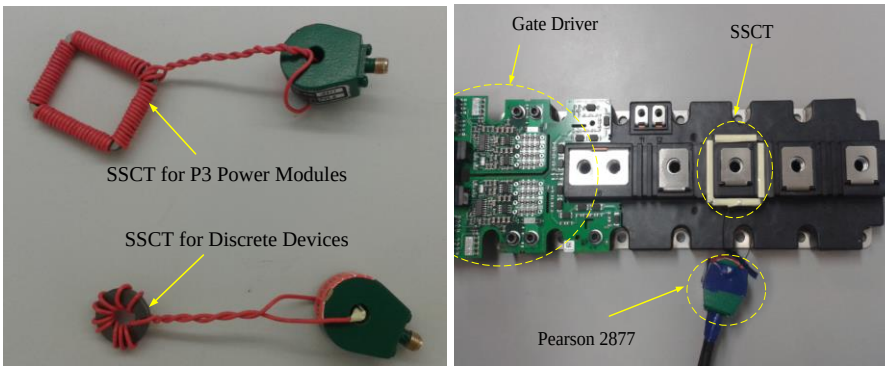


Figure 2.15 Two stage current measurement method with SSCTs

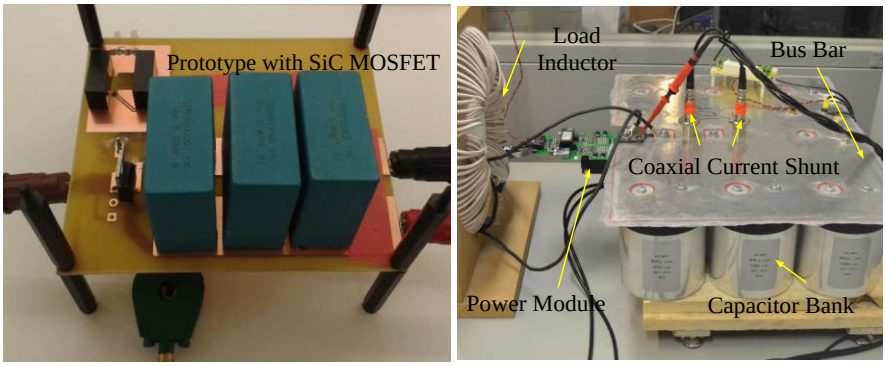


Figure 2.16 Hardware prototyes for evaluation of current measurement with SSCT

The current measurement experiment results of the SiC MOSFET are shown in Figure 2.17. The current measurement experiment results of the high current power module are shown in Figure 2.18.

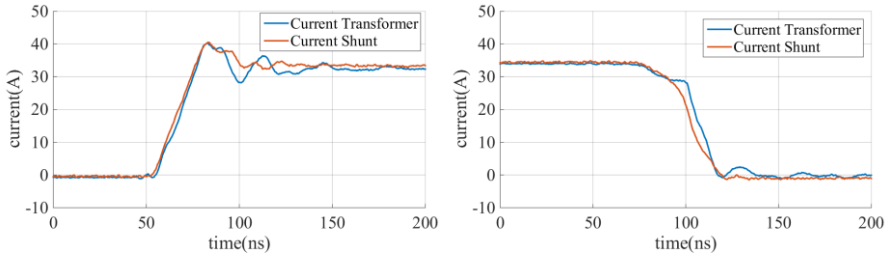


Figure 2.17 Discrete SiC MOSFET current measurement comparisons between using SSCT and current shunt

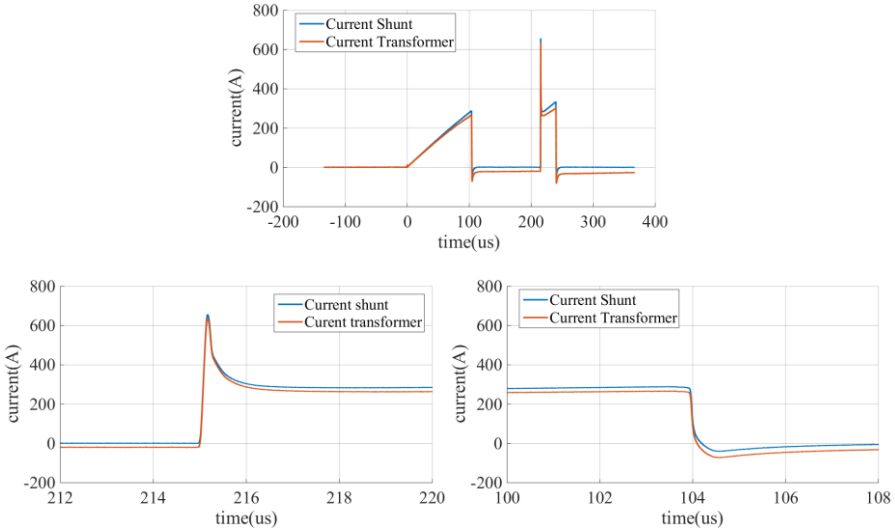


Figure 2.18 Si IGBT power module current measurement comparisons between using SSCT and current shunt

From Figure 2.17, the two stage current measurement with SSCT shows more oscillations and a less than 5ns delay during turn-off compare to the coaxial current shunt measurement. From Figure 2.18, the two stage current measurement method with SSCT for the high current power module shows an offset which increases with the time duration. This phenomenon can be explained with the analysis of the current transformer working mechanism. In (2.12), the measurement error depends on the pulse duration time. The 100μs current rise time is not short enough to be ignored. Therefore, during turn-on and turn-off, there is a measurement offset compare to the measurement with the coaxial current shunt. The turn-on and turn-off

transients are quite short. Therefore, the values of the turn-on current and the turn-off current have little difference with the coaxial current measurement. If the offset is compensated, the current measurement comparison is shown in Figure 2.19. The compensation can be done just by lifting the off-state current to zero in the oscilloscope.

The two stage current measurement with SSCT has more flexibility compared to the measurement with ferrite core current transformer. The size and the shape of the SSCT can be designed and cut aribitrialy. Moreover, with the experimental study, the two stage current measurement with SSCT is capable of measuring high current for characterizatin of the high current power modules.

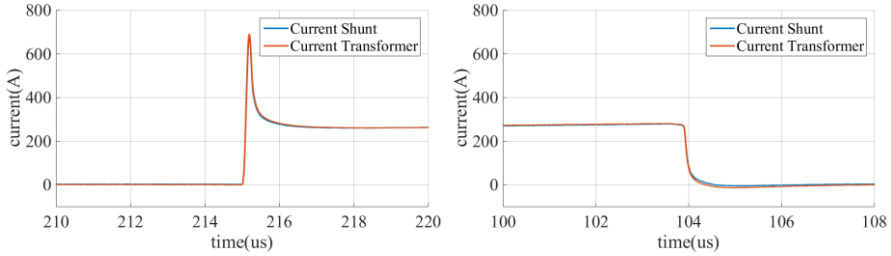


Figure 2.19 Si IGBT power module current measurement comparisons between using SSCT and current shunt after calibration

2.3 SiC MOSFETs switching characterization

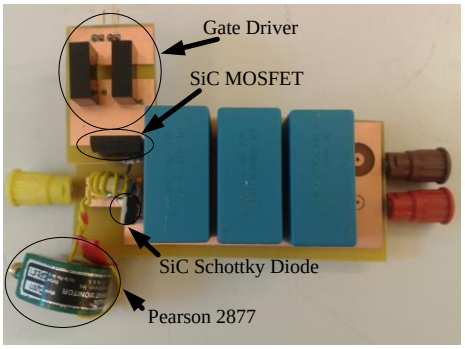


Figure 2.20 Hardware prototype of the double pulse test circuit

For the experiment study of the SiC MOSFET switching characterization, the current measurement is with the two stage current measurement method

with the ferrite core current transformer and the Pearson current monitor 2877. The hardware prototype of the double pulse test circuit is shown in Figure 2.20.

There are some efforts in making this hardware prototype to achieve a clean switching waveform of the SiC MOSFET (C2M0080120D).

First, the switching loop stray inductance is optimized in several steps. The DC link capacitor is put just next to the SiC MOSFET. Besides it, there are some small ceramic capacitors to further reduce the current switching loop area. The freewheeling diode is as close as possible to the drain pin of the SiC MOSFET. The distance is for the current measurement with the two stage current measurement method with the ferrite core current transformer.

Secondly, the common source stray inductance is mitigated by the 'Quasi-Kelvin Source' connection, as shown in Figure 2.21 (a). The gate driver source connection is connected to the end of the source pin. With the TO-247-3 Package, the Quasi-Kelvin Source connection is the most optimal way to reduce the common source stray inductance. The effect of the Kelvin-Source connection has been studied by Infineon [62].

Figure 2.21 (b) shows the load inductor with the single winding layer. Figure 2.22 (c) is the equivalent circuit model of an inductor. C_{pL} is the equivalent paralleled capacitance of the inductor. With the single layer winding inductor, the equivalent paralleled capacitance of the inductor is smaller compared to that of the multi-winding-layer inductors. SiC Schottky diode, which has no reverse recovery current, is used as the freewheeling diode.

(a) (b) (c)

Figure 2.21 Parasitic parameters mitigation (a) Quasi-Kelvin source (b) single winding layer inductor (c) inductor model

With these above mitigation methods, the switching waveforms are shown in Figure 2.22. With a 20Ω gate resistance, the SiC MOSFET has an around 17ns current rise time. The turn-off voltage has a 42.2V voltage dip before the current stop increasing, which is caused by the switching loop stray inductance. The turn-on current speed is 1.46A/ns. With (2.2), the switching loop inductance of the hardware prototype is around 28.9nH. The turn on current still has an overshoot, which is caused by the junction capacitance of the diode and C_{pL}.

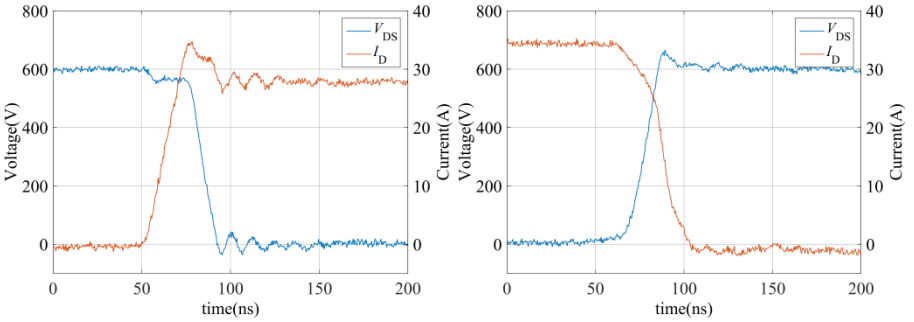


Figure 2.22 Experimental switching waveforms of SiC MOSFET

With different gate resistance from 2Ω-20Ω, the switching behavior of the SiC MOSFET is shown in Figure 2.23.

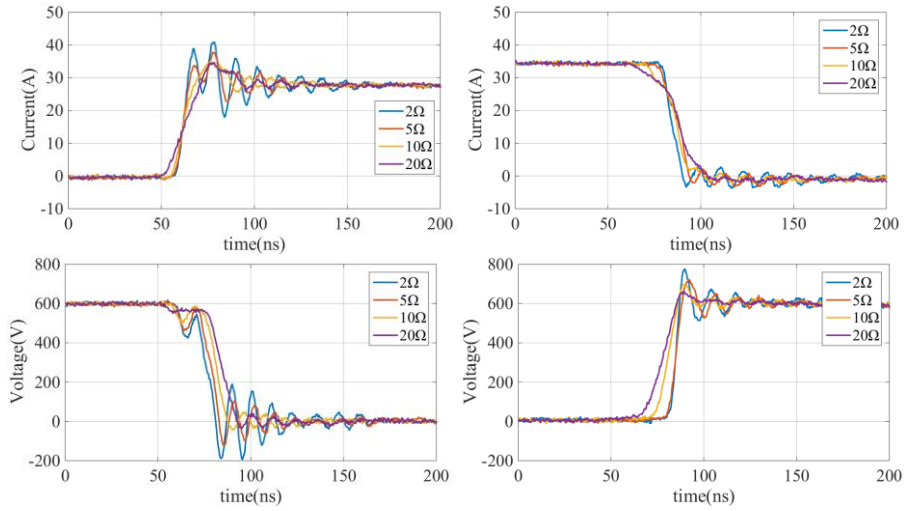


Figure 2.23 Experimental switching behavior with different gate resistors

It is obvious that with a smaller gate resistance, the switching speed of the SiC MOSFET is faster. Compared the switching waveforms with 2Ω to that with 20Ω gate resistance, the current switching speed with 2Ω gate resistance is around 4.02A/ns, which is almost 3 times faster than that with 20Ω gate resistance. The switching losses analysis regarding the gate resistance is presented in Figure 2.24. With a smaller gate resistance, the switching speed is fast and thereby leading to smaller switching losses. However, with the identical parasitic circuit parameters (L_d, L_s and C_p), it is also obvious that a higher switching speed may lead to severe oscillations in the switching waveforms.

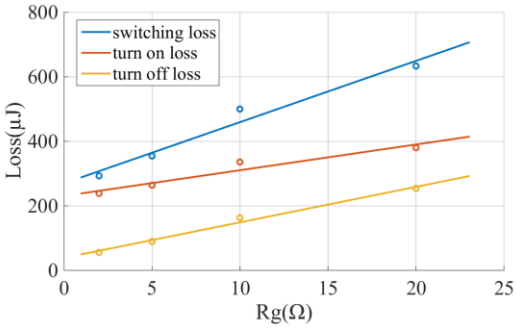


Figure 2.24 Experimental switching losses analysis with gate resistance variation

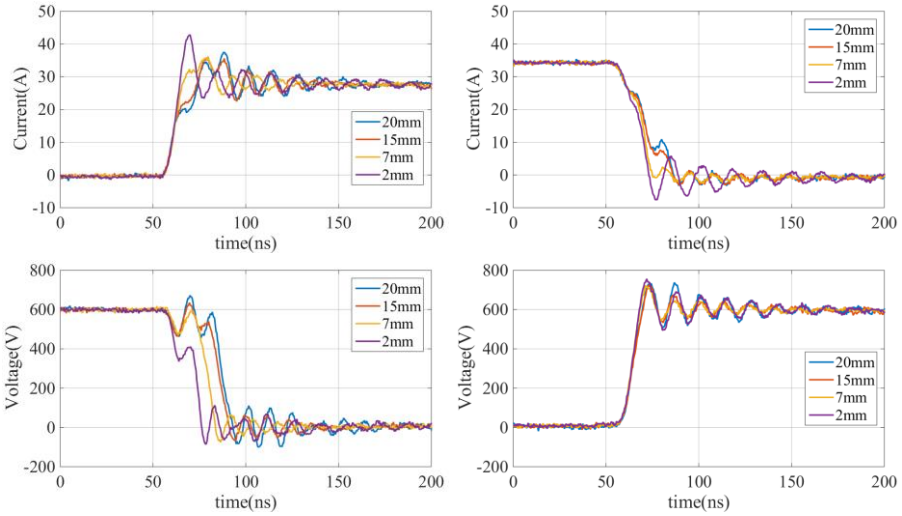


Figure 2.25 Experimental switching behavior with different L_s

The influence of the common source stray inductance is investigated. The common source stray inductance is from the TO-247-3 package. The effective source pin length of the TO-247-3 package, which is connected both in the gate current loop and the power current loop, is adjusted from 2mm to 20mm. The experimental results are presented in Figure 2.25. With the increase of the common source stay inductance, the current switching speed decreases and the delay of the turn-on drain source voltage increases. The common source stray inductance has little influence on the turn-off drain source voltage, which has also been performed with the simulation results. The switching losses analysis with different effective source pin length is summarized in Figure 2.26. Both the turn-on loss and the turn-off loss increase with the increase of the common source stray inductance. The turn-on loss has a higher increasing slope than the turn off loss. That is because the common source stray inductance does not affect the turn-off drain source voltage switching behavior.

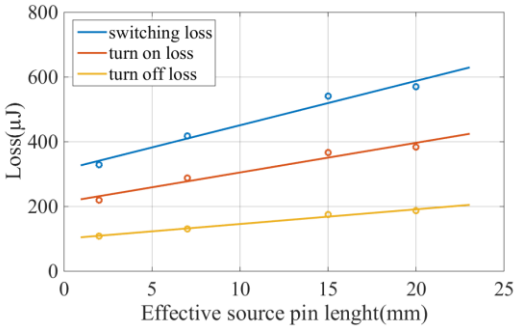


Figure 2.26 Experimental switching losses analysis regarding L_s variation

The switching loop stray inductance is adjusted by inserting the air-core inductors with different turns. The switching behavior with different switching loop stray inductance is shown in Figure 2.27. With the increase of the switching loop stray inductance, the turn-on drain source voltage dip and the turn-off drain source voltage overshoot increase. Therefore, the turn-on loss decreases while the turn off loss increases with the increase of the switching loop stray inductance. The current and voltage oscillations magnitude in the switching waveforms increases while the oscillation frequency decreases with the increase of the switching loop stray inductance. The experiment results match with the simulation results. The switching

losses analysis regarding different switching loop stray inductance is shown in Figure 2.28. According to (2.2), the switching loop stray inductance is calculated with the switching waveforms in Figure 2.27.

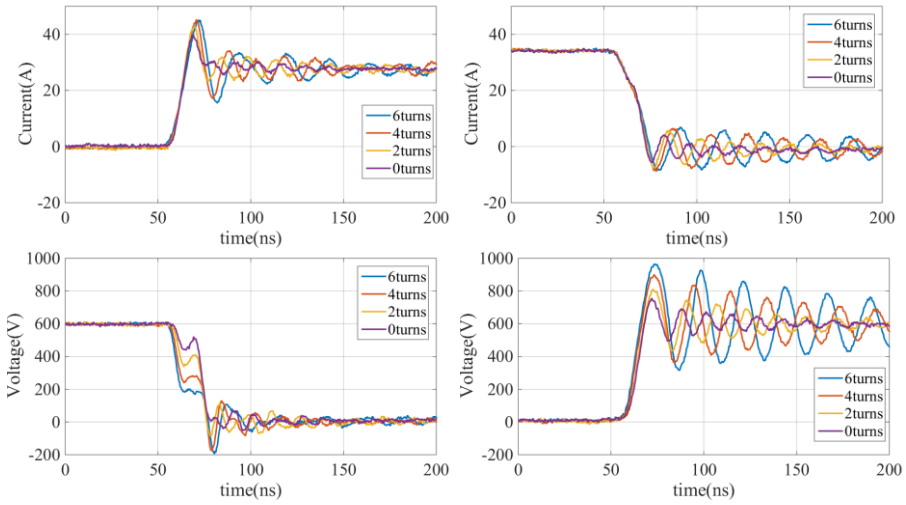


Figure 2.27 Experimental switching behavior with different L_d

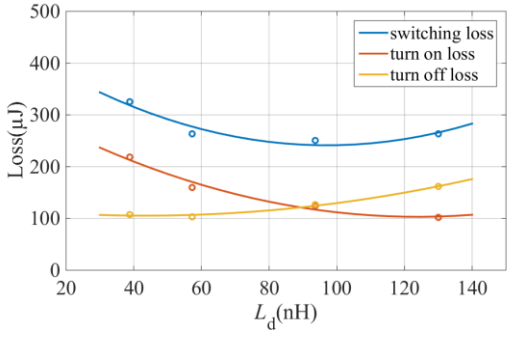


Figure 2.28 Experimental switching loss analysis regarding L_d variation

2.4 Conclusion

This chapter makes the switching characterziation of the SiC MOSFET. The present pulse current measurement methods for characterization of fast switching power semiconductors are compared regarding the performance of high frequency bandwidth, galvanic isolation and mechanical size. The merits and drawbacks of the present current measurement methods are summaried: coaxial current shunt does not have galvanice isolation, pearson

current monitor has a large physical size and the rogowski ciol has a low band width. The proposed two stage current measurement method with silicon steel current transformer aviod the physical size limitation of the pearson current monitor. The influences of the gate resistance and the circuit parasitic parameters on the switching behavior are investigated with LTspice simulation and experimental study. The switching losses analysis are summarized according to the experimental switching behaviors of the SiC MOSFET. The TO-247 package for SiC MOSFET may have large parasitic inductance. To fully utilize the fast switching speed of SiC MOSFET, the common source stray inductance of package need to be minimized in the application.

3 Influence of device and circuit mismatch on paralleling SiC MOSFETs

Parallel connection of power semiconductors, e.g. Si MOSFET and Si IGBT, is not a new topic, either paralleling discrete packaged devices or paralleling bare dies in multichip power modules. The aim of the parallel connection is to improve the current capability of the power semiconductors due to the limitation of the single die size. The undesirable issue of the parallel connection is the current imbalance among the paralleled devices, which including the steady state current imbalance and the transient switching current imbalance. The causes of the current imbalance may be the mismatch of the power semiconductor device parameters and the mismatch of the circuit parameters.

At present, SiC MOSFET has a less mature fabrication process compared with the Si counterpart. Therefore the single die size of the SiC MOSFET is even smaller than Si devices. Consequently, the parallel connection of the SiC MOSFET is more desirable in high current applications. On the other hand, the SiC MOSFET is expected to switch much faster than Si IGBT. The sensitivity of the SiC MOSFET to the circuit parasitic parameters is, therefore, much higher than that of the Si IGBT. In this chapter, the influences of the SiC MOSFET device parameters mismatch and the circuit parameters mismatch are discussed. Mathematic analysis about the circuit mismatches is presented. Experimental results validate the analysis and give the current sharing performance with specific device mismatches or circuit mismatches.

3.1 Device parameters mismatch

3.1.1 Device mismatch description

Among the device parameters of SiC MOSFETs, the on-state resistance (R_{on}) and the threshold voltage (V_{th}) are the two most critical parameters that affect the current sharing performance in the parallel connection. R_{on} determines the on-state current distribution, whereas V_{th} influences the sharing of transient current.

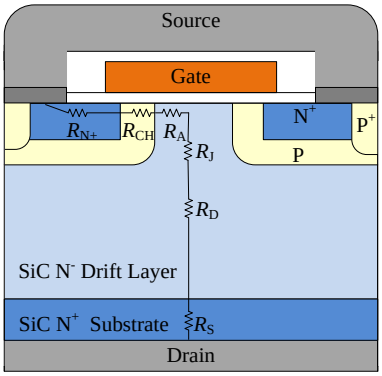
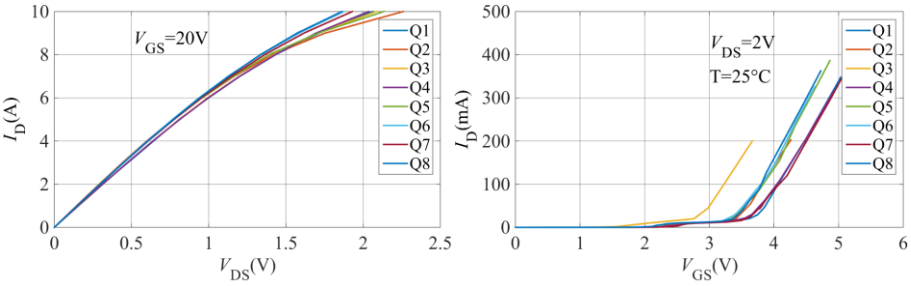


Figure 3.1 A cross-section schematic of unit cell for planar SiC MOSFET

Figure 3.1 shows a cross-section schematic of a unit cell for the planar SiC MOSFET [63], which is similar to that of Si MOSFET [64]. Compared to Si MOSFETs, SiC MOSFETs have a lower drift region resistance (R_D), but a higher channel resistance (R_{CH}), due to its lower carrier mobility [63] and a higher level of the channel defect density, which also contributes to the overall on-resistance. At the low gate-source voltages (u_{GS}<13V), R_{CH} dominates the total R_{on}, which has a negative temperature coefficient. Hence, it is always recommended to turn on SiC MOSFETs with u_{GS} higher than 18V [63, 65]. Otherwise, paralleling SiC MOSFETs does not have a self-balancing capability and there is a risk of thermal run away.

From semiconductor physics, it is known that the threshold voltage V_{th} of the MOS structure is affected by non-idealities, which can lead to shifts in the threshold voltage during long term of cycling. Such non-idealities can be oxide trap states that contain fixed charges or interface states, which are imperfections at the atomic level at the boundary between the oxide and the SiC [66]. Moreover, the material processes of SiC are not as mature as Si, the manufacturing process and the interface quality remains a material issue [67, 68], although this is being addressed by improving material processing, like nitridation of the gate oxide [69-72]. As a consequence, slight synthesis variations in the processing may lead to process related variations in the interface and oxide quality, with a variation in threshold voltage as a result. Therefore, SiC MOSFETs are more likely to operate with V_{th} mismatch, especially after long term of cycling.

3.1.2 Device parameters test and hardware setup

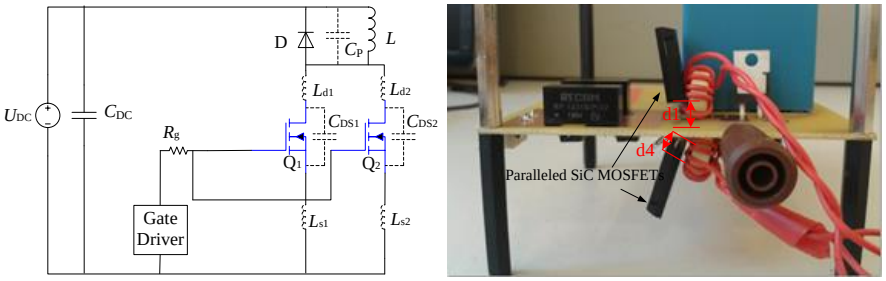


(a) (b)

Figure 3.2 SiC MOSFETs Q_1-Q_8 parameters (a) R_{on} (b) V_{th}

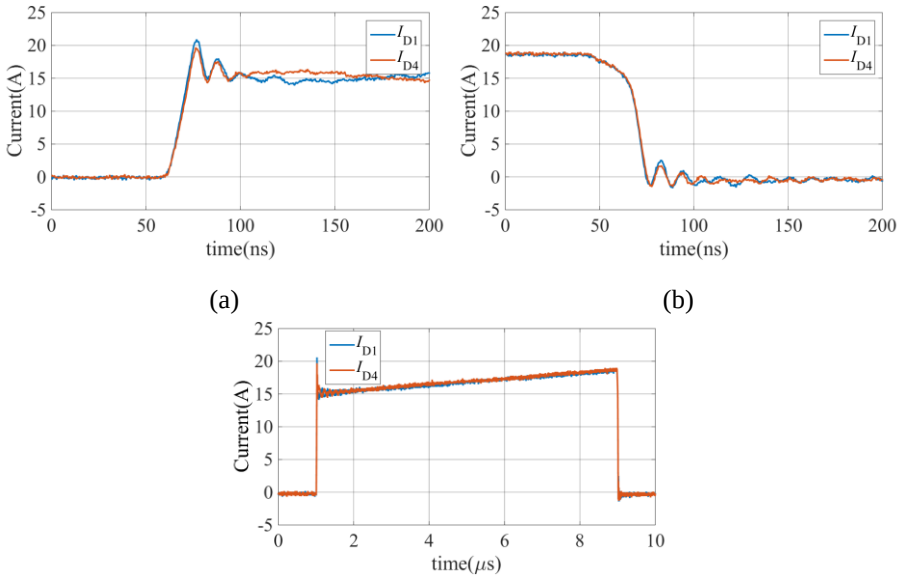
To demonstrate the effect of device mismatch, 8 SiC MOSFETs (C2M0160120D) from Cree are tested in the lab. They are denoted as Q_1-Q_8. R_{on} and V_{th} variations of these devices are plotted in Figure 3.2. The procedure of measuring R_{on} variation is summarized as the following. First, the gate source voltage is kept constant at 20V. The drain and the source terminals are connected to a power supply, which operates in the current source mode and is adjusted from 0 to 10A. The MOSFETs are mounted on a heatsink with fan cooling. Then, the drain source voltage u_{DS} is measured after u_{DS} becomes stable. Even though there is self-heating effect during the testing procedure, the R_{on} variation of the MOSFETs can still be demonstrated under the almost same testing condition.

The current sharing of paralleling SiC MOSFETs is evaluated with a double pulse test circuit, as shown in Figure 3.3(a). The hardware implementation is shown in Figure 3.3(b). In the simulation and experimental study in this paper, the gate source voltage bias is 24V and -5V unless otherwise specified. Since the device mismatch is of the main concern in this test, two SiC MOSFETs are paralleled in a flipped way, as shown in Figure 3.3(b), in order to reduce the influence of circuit mismatch. The MOSFET drain current is measured with a two stage current measurement method, which includes a 10-turns current transformer at the first stage and a Pearson Current Monitor 2877 in the second stage [61].



(a) (b)

Figure 3.3 Two SiC MOSFETs in parallel connection. (a) Double pulse test circuit (b) hardware setup



(a) (b)

(c)

Figure 3.4 Current sharing of Q_1 and Q_4 (a) turn on (b) turn off (c) on state

Figure 3.4 shows current sharing of the paralleled Q_1 and Q_4, which have little device parameters mismatch and minimized circuit mismatch with flipped connection. A good current sharing performance is obtained, which can be seen as a benchmark for the following tests.

3.1.3 Influences of on-Resistance mismatch

SiC MOSFETs Q_1 and Q_7 are used for the study of R_{on} mismatch influence, as they have nearly same V_{th} but different R_{on}, Q_1 has a higher R_{on} than Q_7.

As shown in Figure 3.5(a), during turn-on transient, Q_1 and Q_7 have identical current. After the turn-on, Q_1 has lower current than Q_7. Q_1 has lower on-state current because of its higher R_{on}, as shown in Figure 3.5(c). It is confirmed that the R_{on} mismatch has an impact on on-state current sharing performance but little influence on transient current sharing.

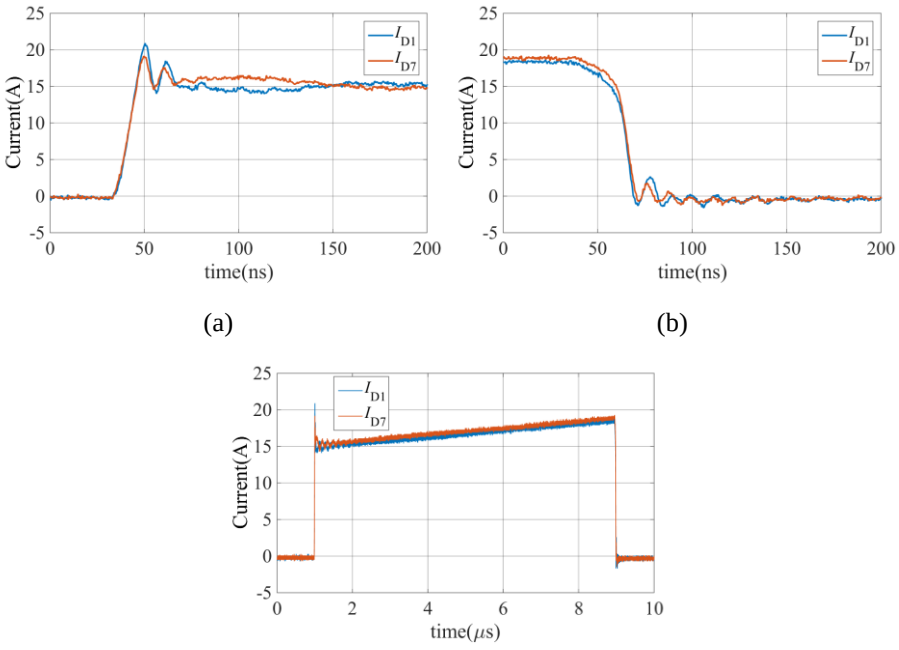


Figure 3.5 Current sharing of Q_1 and Q_7 (a) turn on (b) turn off (c) on state

3.1.4 Influences of threshold voltage mismatch

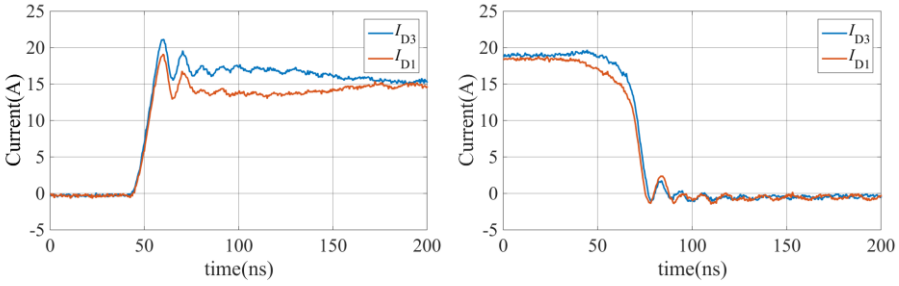


Figure 3.6 Current sharing of Q_1 and Q_3

Q_1 and Q_3 are selected for the study of V_{th} mismatch influence, as they have nearly identical R_{on} but different V_{th}. Q_1 has a higher V_{th} than Q_3. The switching transient current sharing of Q_1 and Q_3 is given in Figure 3.6.

Q_3 turns on faster yet turns off slower than Q_1. During turn-on, u_{GS} first reach V_{th} of Q_3, and then Q_3 starts to turn-on and i_{D3} starts rising. When u_{GS} continue increasing and reaches V_{th} of Q_1, Q_1 turns on and i_{D1} starts rising.

However, during turn-off, the process is slightly different. The minimum gate source voltage maintaining the specific drain current is defined as V_p. If the reduced u_{GS} is still larger than V_p, the drain current will not fall and the channel resistance of the SiC MOSFET will increases. Only if u_{GS} keeps decreasing to be lower than V_p, the SiC MOSFET will start to work in the saturation region, and the drain current will be determined by u_{GS}. u_{GS} first decreases to the point V_{P1}, at which Q_1 cannot sustain its drain current. i_{D1} starts to decrease. u_{GS} continues falling to the point V_{P3}, at which Q_3 can no longer sustain i_{D3}, and then i_{D3} starts decreasing. Since the drain current i_D is determined by u_{GS} in the saturation region, as (3.1),

$$i_D = g_{fs}(u_{GS} - V_{th}) \tag{3.1}$$

$V_{th1}>V_{th3}$, trans-conductance of these two SiC MOSFET $g_{fs1}=g_{fs3}$ and on-state current $i_{D1}=i_{D3}$ before turning off, $V_{P1}>V_{P3}$. As i_{D1} first decreases but the load inductor current i_L keeps unchanged and the diode is not conducted, Q_3 needs to handle more current. Therefore, during turn-off, i_{D3} first increases small amplitude before it starts decreasing, as shown in Figure 3.6(b).

3.2 Circuit mismatch

3.2.1 Circuit mismatch description

The difference in switching loop stray inductance (L_d) and common source stray inductance (L_s) are the main causes of current unbalance due to circuit mismatch, as shown in Figure 3.3(a). L_{d1} and L_{d2} represent switching loop stray inductance. L_{s1} and L_{s2} are the common source stray inductances. C_P is the total capacitance of the diode junction capacitor and the parasitic paralleled capacitor of load inductor. C_{DS1} and C_{DS2} are junction capacitance of Q_1 and Q_2. The switching loop stray inductance includes the equivalent-series-inductor (ESL) of the dc-link capacitors, the stray inductance of the

power connection, including PCB trace and partial inductance from the package of power devices. The common source stray inductance is mainly from the package of SiC MOSFETs and PCB trace which is both in the gate-source loop and drain-source loop. The mismatch of L_d and L_s can easily be increased in the case of paralleling more than two SiC MOSFETs, where an ideally symmetric layout is difficult to achieve, especially when a large heat sink is needed.

In the study of circuit mismatch influence, Q_1 and Q_4 are selected as they have little device parameter mismatch. The L_s mismatch is realized by different effective source pin length, as shown in Figure.3 (b). d_1 and d_4 are the effective source pin length for Q_1 and Q_4. L_d mismatch is by inserting different small air core inductors in the drain connection.

3.2.2 Influences of common source stray inductance mismatch

L_s affects the switching characteristics by its negative feedback effect on u_{GS}, which can be explained with (3.2)-(3.3) during saturation region in transient switching time. In this condition, SiC MOSFET source current i_s is considered identical with drain i_D, because gate source current is much smaller than the i_D.

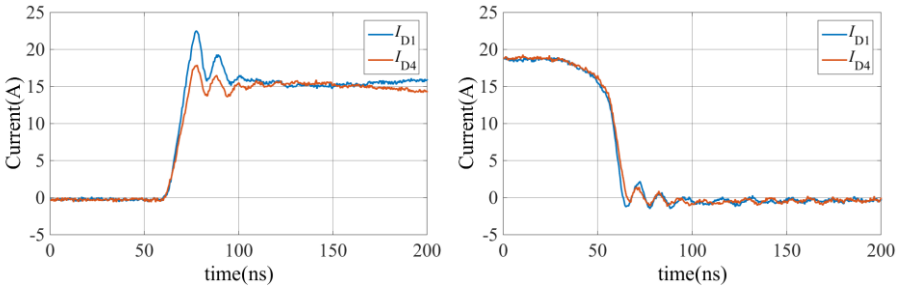
$$u_{GS} = V_{driver} - i_G R_G - L_s \frac{di}{dt} \tag{3.2}$$

$$i_{D1} - i_{D2} = g_{fs}(L_{s2} - L_{s1}) \frac{di_L}{dt} \tag{3.3}$$

According to (3.2) and (3.3), during turn-on transient, the SiC MOSFET with larger L_s turns on slower and takes less current compared to the one with smaller L_s. During turn-off transient, the SiC MOSFET with larger L_s turns off slower but takes more current.

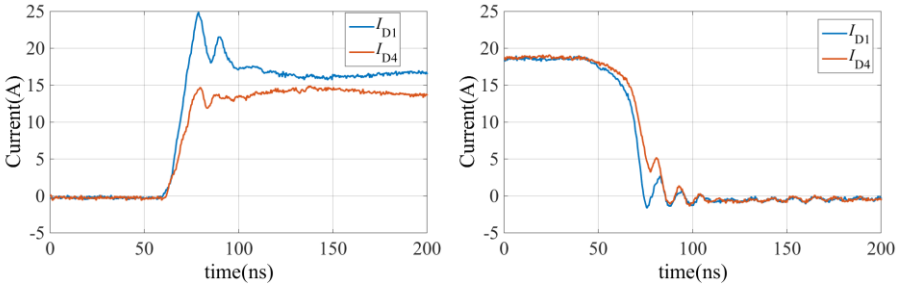
Figure 3.7 and Figure 3.8 show the L_s mismatch influence on the current sharing performance of paralleled SiC MOSFETs. The L_s mismatch is adjusted by changing the effective source pin lengths, which are specified as d_1 and d_4 in Figure 3.2 (b). d_1 and d_4 are the source pin length connected to the power loop, i.e. the distance from the PCB trace to the end of the source pin, which can be readily adjusted by lifting the MOSFET up and down with different distances. With L_s mismatch increased, the current unbalance

during switching transient also increases. For the SiC MOSFET with larger L_s, both the processes of turn-on and turn-off become slower. The current overshoot of the SiC MOSFET with smaller L_s increases with the increase of L_s mismatch. The current unbalance leads to uneven turn-on and turn-off loss during switching transient.



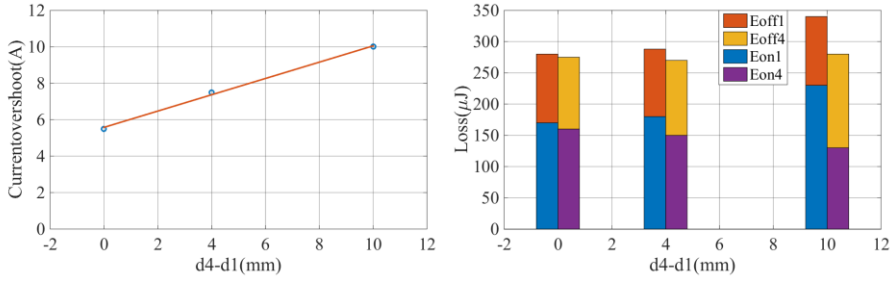
(a) (b)

Figure 3.7 Current sharing of Q_1 and Q_4 with d_1=6mm and d_4=10mm



(a) (b)

Figure 3.8 Current sharing of Q_1 and Q_4 with d_1=6mm and d_4=16mm



(a) (b)

Figure 3.9 Current overshoot and switching losses analysis with L_s mismatch (a) current overshoot analysis (b) switching loss analysis

The current overshoot and switching loss analysis are shown in Figure 3.9 for different values of (d_4-d_1). E_{on} and E_{off} are SiC MOSFET turn-on loss and turn-off losses. It can be seen from Figure 3.9(a) that the current overshoot of the SiC MOSFET increases with the increase of L_s mismatch. On the other hand, L_s mismatch has little effect on the on-state current sharing performance since it affects the current sharing performance through u_{GS}.

3.2.3 Influences of switching loop stray inductance mismatch

The capacitor C_P shown in Figure 3.3(a) could lead to a current overshoot during turn-on transient. L_d and C_P form a resonant circuit and causes oscillations in a short period after turn-on. The oscillation frequency could be determined as (3.4). For the oscillation, R_{on} of SiC MOSFET in series with the equivalent series resistance (ESR) of the dc-link capacitors (R_C) acts as the damping resistor and the damping factor ξ is given by (3.5).

$$f=\frac{1}{2\pi\sqrt{L_d C_P}} \tag{3.4}$$

$$\xi=\frac{(R_{on}+R_C)}{2\pi}\sqrt{\frac{C_P}{L_d}} \tag{3.5}$$

During turn-off, there is a current charging the drain-source capacitor (C_{DS}) of SiC MOSFET. In a short period after turn-off, L_d and C_{DS} form a resonant circuit and the oscillation frequency could be determined as (3.6). Damping resistor for this oscillation is ESR of DC capacitors and the ESR of diode (R_d). Damping factor ξ is as (3.7).

With the above analysis, L_d has an influence on the current in a short period after turn-on and turn-off. SiC MOSFET with larger L_d has smaller oscillation frequency and smaller damping factor after turn-on and turn-off. As a result, the SiC MOSFET with larger L_d has a larger current overshoot and the current oscillation amplitude after turn-off is also larger.

$$f=\frac{1}{2\pi\sqrt{L_d C_{DS}}} \tag{3.6}$$

$$\xi=\frac{(R_{\mathrm{d}}+R_{\mathrm{C}})}{2\pi}\sqrt{\frac{C_{\mathrm{P}}}{L_{\mathrm{d}}}} \tag{3.7}$$

Besides L_{d} mismatch influences on the transient period current sharing performance, mismatch of L_{d} also has an impact on the on-state current distribution. During on-state, there are cases that the SiC MOSFETs see an inductive load current and i_{D} has a changing slope. During on-state period, the equivalent power circuit is shown as Figure 3.10. The drain current can be described with (3.8). In condition of $R_{\mathrm{on1}}=R_{\mathrm{on2}}$ and $\mathrm{d}i_{\mathrm{D1}}/\mathrm{dt}=\mathrm{d}i_{\mathrm{D2}}/\mathrm{dt}$ (determined by load), the current difference of i_{D1} and i_{D2} can be determined as (3.9), which means different L_{d} lead to different on-state current. Larger L_{d} results smaller on-state current.

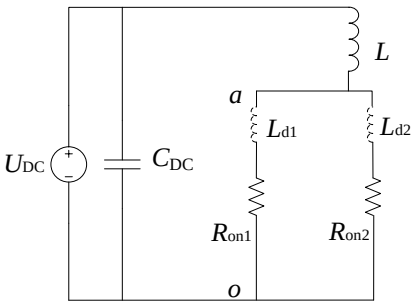


Figure 3.10 On-State equivalent circuit of paralleling two SiC MOSFETs

$$\begin{cases} i_{\mathrm{D1}}+i_{\mathrm{D2}}=i_{\mathrm{L}} \\ L\dfrac{\mathrm{d}i_{\mathrm{L}}}{\mathrm{d}t}+u_{\mathrm{ao}}=U_{\mathrm{DC}} \\ L_1\dfrac{\mathrm{d}i_{\mathrm{D1}}}{\mathrm{d}t}+R_{\mathrm{on1}}i_{\mathrm{D1}}=L_2\dfrac{\mathrm{d}i_{\mathrm{D2}}}{\mathrm{d}t}+R_{\mathrm{on2}}i_{\mathrm{D2}} \end{cases} \tag{3.8}$$

$$i_{\mathrm{D1}}-i_{\mathrm{D2}}\approx\frac{L_{\mathrm{d2}}-L_{\mathrm{d1}}}{2R_{\mathrm{on}}}\frac{U_{\mathrm{DC}}}{L} \tag{3.9}$$

The experiment of L_{d} mismatch influence is realized by inserting a small inductors in the drain of SiC MOSFET Q_1. The experiment results are shown in Figure 3.11 and Figure 3.12. With the increase of L_{d}, the current oscillation frequency decreases but the oscillation amplitude increases. With the increases of L_{d} mismatch, on-state current unbalance increases.

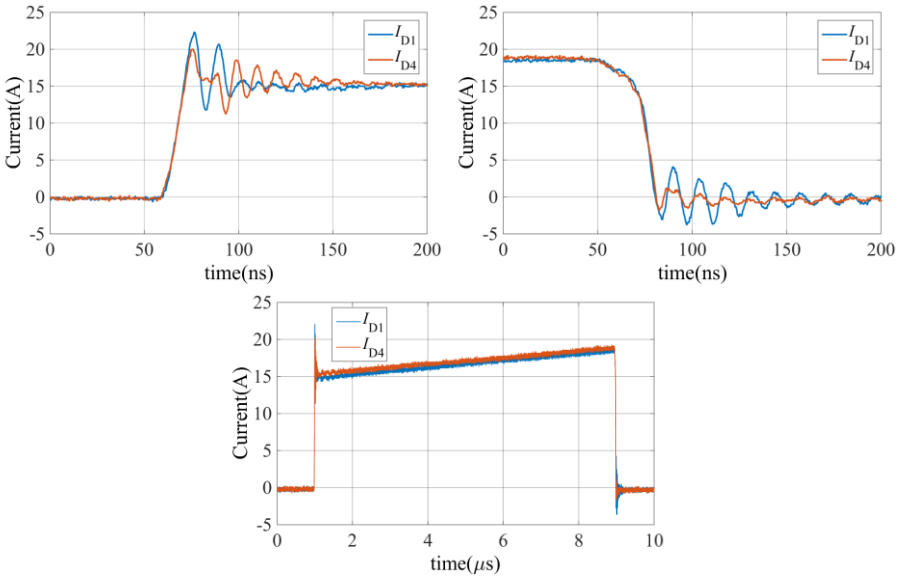


Figure 3.11 Current sharing of Q_1 and Q_4. L_{d1}-L_{d4}=66nH

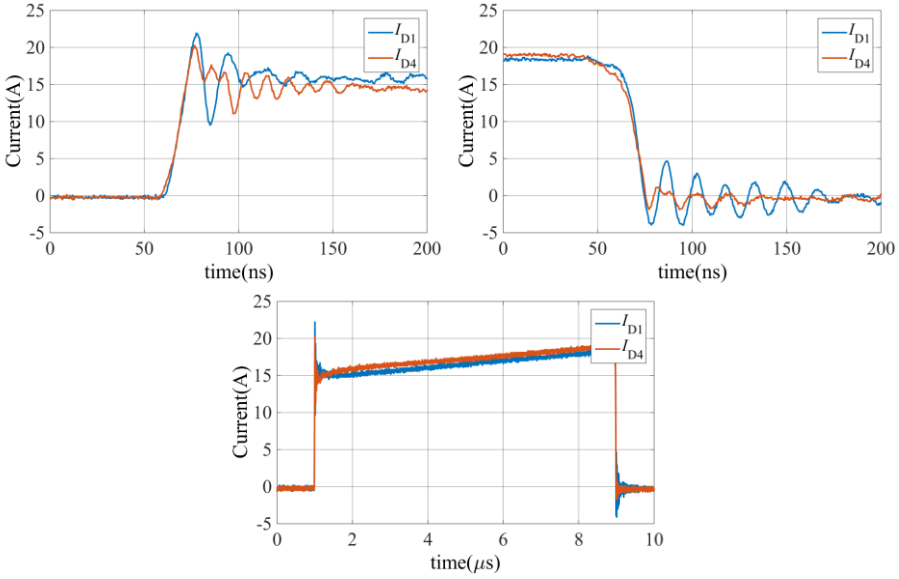


Figure 3.12 Current sharing of Q_1 and Q_4. L_{d1}-L_{d4}=140nH

Besides the influence on current, L_d has a large impact on the drain source voltage (u_{DS}) during switching transient. The effect of L_d on a single MOSFET u_{DS} has been analyzed in [73, 74]. The conclusion is with the

larger L_d, u_{DS} has larger voltage dip during turn-on and higher voltage overshoot during turn-off, which results a smaller turn-on loss but larger turn-off loss. For the paralleled connection, the experiment results of u_{DS1} and u_{DS4} are given in Figure 3.13 and Figure 3.14. u_{DS} overshoot and switching losses analysis with L_d mismatch are summarized as Figure 3.15.

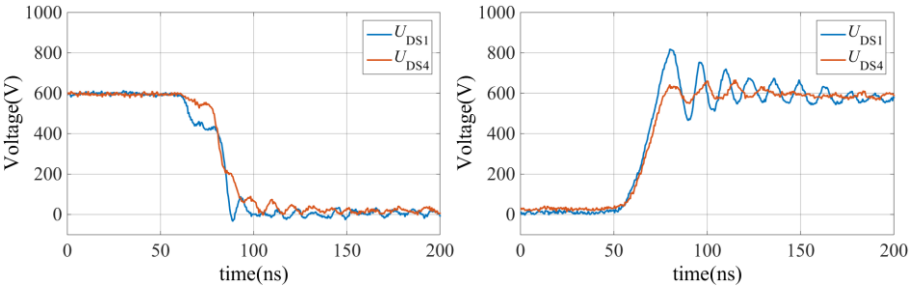


Figure 3.13 Drain-Source voltages of Q_1 and Q_4. L_{d1}-L_{d4}=66nH

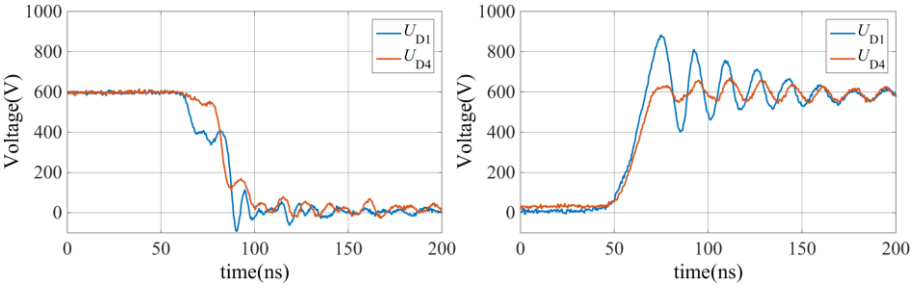
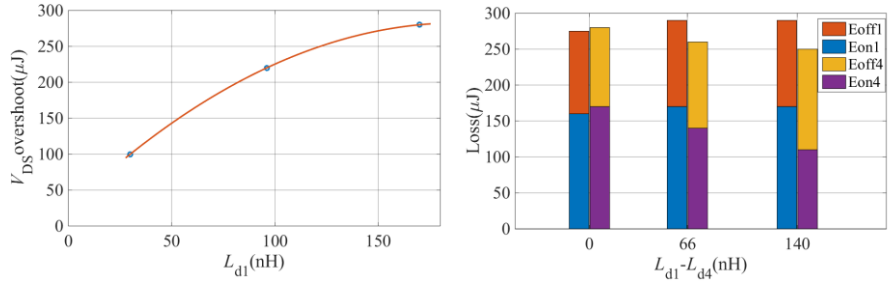


Figure 3.14 Drain-Source voltages of Q_1 and Q_4. L_{d1}-L_{d4}=140nH



(a) (b)

Figure 3.15 Drain-source voltage overshoot and switching losses analysis (a) voltage overshoot analysis (b) switching losses analysis

3.3 Conclusion

This chapter discusses the influences of the device and circuit mismatches on the parallel connection of SiC MOSFETs. The mismatches of the device parameters, R_{on} and V_{th}, are experimentally investigated. The influences of the circuit mismatches regarding the switching loop stray inductance mismatch and the common source stray inductance are mathematically analyzed and experimentally studied. It is found that the mismatch of the switching loop stray inductance can lead to on-state current unbalance in case of the load current is inductive. The mismatch of the common source stray inductance, on the other hand, causes transient current unbalance due to the negative feedback effect of the common source stray inductance on the gate source voltage. Based on the experimental study, the current and voltage overshoot and the switching losses are analyzed in relation to the circuit stray inductances.

4 Paralleling SiC MOSFETs in multichip power modules

Multichip power modules with paralleled power semiconductor dies are widely used in high current applications, e.g. the wind power systems and the traction systems. In the multichip power modules with paralleled dies, the uniform current distribution among the paralleled dies is desirable, as the non-uniform current distribution can lead to thermal imbalance and low ruggedness of the power module [47, 48].

For the parallel connection of Si MOSFETs, the influence of the device parameters (R_{on} and V_{th}) mismatch on the current sharing performance was discussed by J.B. Forsythe [46]. For the parallel connection of Si IGBTs, the device parameters (V_{CE} and V_{th}) were also studied in some papers. For the parallel connection of SiC MOSFETs, the influence of the device and circuit mismatches on the current sharing performance was discussed in Chapter 3. Regarding the influences of the circuit mismatch in the power module, Consoli, et al. [52] presented the influences of the internal layout of the power modules with paralleled IGBT dies. Takeshi et al. [49] investigated the bus bar structure influences on the current distribution in the IGBT power modules. Both of them showed the non-uniform transient current distribution among the paralleled Si IGBT dies in the power module. Regarding the power modules with paralleled SiC devices, the non-uniform current distribution was also presented [75]. However, the current imbalance, especially the transient current imbalance, has not been fully understood with the published research works. Consequently, in the limited DBC board area, the DBC layout design is not optimized for the current sharing and the power modules are usually de-rated. The most critical part is that the non-optimal design is not even realized: which is the non-optimal part and how to optimize the design.

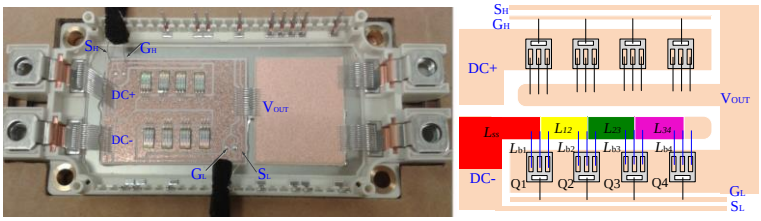
This chapter discusses the influences of the DBC layout on the current distribution among the paralleled SiC MOSFET dies in the power modules. It reveals that there is a circuit mismatch in the DBC layout of the presented SiC MOSFET power module. The mismatch of the common source stray inductance among the paralleled dies causes the transient current imbalance

in the power module. Moreover, a current coupling effect, which aggravates the current imbalance, is uncovered in the DBC layout. Successively, the DBC layout with auxiliary source bond wires is investigated. The merits and the drawbacks with the auxiliary source bond wires are discussed for the first time. The current stress on the auxiliary source bond wires is mathematically analyzed. A method of extracting the parasitic parameters in the power module is explored using Ansys Q3D. Simulations and experimental results are presented to validate the analysis.

4.1. Mathematic analysis of the DBC layout

A half bridge power module with paralleled SiC MOSFET dies is shown in Figure 4.1(a). The power module is made by Danfoss and dedicated for the DBC testing. The DBC layout of the power module is shown in Figure 4.1(b). The power module has a symmetric DBC layout for the top four MOSFETs and the bottom four MOSFETs. The research point is the current sharing performance among the paralleled dies. Therefore, the bottom DBC layout is studied as an example.

In Figure 4.1(b), the parasitic inductance of the bond wires and the DBC traces are highlighted in different colors. Q_1-Q_4 are the bottom four SiC MOSFETs. L_b is the parasitic inductance of the bond wires for the source connection. L_{ss} is the stray inductance of the DBC trace (red) from Q_1 to DC- terminal. L_{12}, L_{23} and L_{34} are the stray inductance of the DBC trace between Q_1 and Q_2 (yellow), Q_2 and Q_3 (green), Q_3 and Q_4 (purple), respectively. In the DBC layout, L_{12}=L_{23}=L_{34}=L_M, L_{b1}=L_{b2}=L_{b3}=L_{b4}=L_b. Following Figure 4.1(b), the model of the DBC layout with the stray inductances in a double pulse test circuit is shown in Figure 4.2.



(a) (b)

Figure 4.1 SiC MOSFET power module and DBC layout (a) SiC MOSFET power module (b) DBC layout

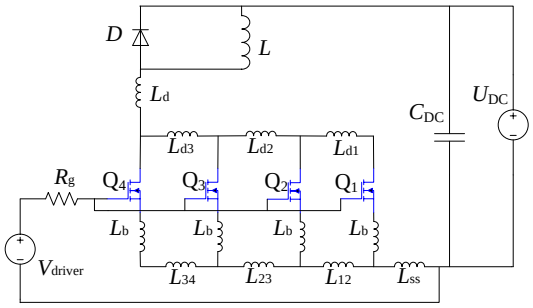


Figure 4.2 Model of the bottom four paralleled SiC MOSFET layout

As discussed in chapter 2 and chapter 3, for the MOSFETs, there are two types of stay inductances affecting the switching performance. One is the switching loop stray inductance (L_d) and the other one is the common source stray inductance (L_s). The common source inductance has a negative feedback effect on the gate source voltage, as shown in (4.1). During the switching transient, the MOSFET drain current is determined by the gate source voltage in the MOSFET saturation region, as show in (4.2).

$$V_{GS} = V_{driver} - i_G R_G - L_s \frac{di_s}{dt} = V_{driver} - i_G R_G - \Delta V_{LS} \tag{4.1}$$

$$i_D = g_{fs}(V_{GS} - V_{th}) \tag{4.2}$$

In Figure 4.2, the common source stray inductances (L_{s1}, L_{s2}, L_{s3} and L_{s4}) for the SiC MOSFET dies (Q1, Q2, Q3 and Q4) are presented in (4.3). As shown in Figure 4.2 and (4.3), the four bottom MOSFETs have different L_s. The common source stray inductance mismatch between the paralleled dies has a large influence on the transient current sharing performance, which has been discussed in chapter 3 [76]. With (4.1) and (4.3), the voltages on the common source stray inductances are calculated in (4.4). Consequently, the drain currents of the MOSFETs in the saturation region during switching transient are determined in (4.5).

$$\begin{cases} L_{s1} = L_{ss} + L_b \\ L_{s2} = L_{ss} + L_{12} + L_b = L_{ss} + L_M + L_b \\ L_{s3} = L_{ss} + L_{12} + L_{23} + L_b = L_{ss} + 2L_M + L_b \\ L_{s4} = L_{ss} + L_{12} + L_{23} + L_{34} + L_b = L_{ss} + 3L_M + L_b \end{cases} \tag{4.3}$$

$$\begin{bmatrix} \triangle V_{\mathrm{LS1}} \\ \triangle V_{\mathrm{LS2}} \\ \triangle V_{\mathrm{LS3}} \\ \triangle V_{\mathrm{LS4}} \end{bmatrix} = \begin{bmatrix} L_{\mathrm{s1}} & L_{\mathrm{ss}} & L_{\mathrm{ss}} & L_{\mathrm{ss}} \\ L_{\mathrm{ss}} & L_{\mathrm{s2}} & L_{\mathrm{ss}}+L_{12} & L_{\mathrm{ss}}+L_{12} \\ L_{\mathrm{ss}} & L_{\mathrm{ss}}+L_{12} & L_{\mathrm{s3}} & L_{\mathrm{ss}}+L_{12}+L_{23} \\ L_{\mathrm{ss}} & L_{\mathrm{ss}}+L_{12} & L_{\mathrm{ss}}+L_{12}+L_{23} & L_{\mathrm{s4}} \end{bmatrix} \begin{bmatrix} i_{\mathrm{D1}} \\ i_{\mathrm{D2}} \\ i_{\mathrm{D3}} \\ i_{\mathrm{D4}} \end{bmatrix} \tag{4.4}$$

$$\begin{bmatrix} i_{\mathrm{D1}} \\ i_{\mathrm{D2}} \\ i_{\mathrm{D3}} \\ i_{\mathrm{D4}} \end{bmatrix} = g_{\mathrm{fs}} \begin{bmatrix} V_{\mathrm{driver}} - i_{\mathrm{g}} R_{\mathrm{g}} - V_{\mathrm{th}} - \triangle V_{\mathrm{LS1}} \\ V_{\mathrm{driver}} - i_{\mathrm{g}} R_{\mathrm{g}} - V_{\mathrm{th}} - \triangle V_{\mathrm{LS2}} \\ V_{\mathrm{driver}} - i_{\mathrm{g}} R_{\mathrm{g}} - V_{\mathrm{th}} - \triangle V_{\mathrm{LS3}} \\ V_{\mathrm{driver}} - i_{\mathrm{g}} R_{\mathrm{g}} - V_{\mathrm{th}} - \triangle V_{\mathrm{LS4}} \end{bmatrix} \tag{4.5}$$

With (4.4) and (4.5), in the saturation region during the transient switching period, the current imbalance among the paralleled dies are as (4.6), under the condition of no device parameters mismatch.

$$\begin{cases} i_{\mathrm{D1}} - i_{\mathrm{D2}} = g_{\mathrm{fs}} \left[L_{\mathrm{b}} \dfrac{\mathrm{d}(i_{\mathrm{D2}} - i_{\mathrm{D1}})}{\mathrm{d}t} + L_{12} \dfrac{\mathrm{d}(i_{\mathrm{D2}} + i_{\mathrm{D3}} + i_{\mathrm{D4}})}{\mathrm{d}t} \right] \\ i_{\mathrm{D2}} - i_{\mathrm{D3}} = g_{\mathrm{fs}} \left[L_{\mathrm{b}} \dfrac{\mathrm{d}(i_{\mathrm{D3}} - i_{\mathrm{D2}})}{\mathrm{d}t} + L_{23} \dfrac{\mathrm{d}(i_{\mathrm{D3}} + i_{\mathrm{D4}})}{\mathrm{d}t} \right] \\ i_{\mathrm{D3}} - i_{\mathrm{D4}} = g_{\mathrm{fs}} \left[L_{\mathrm{b}} \dfrac{\mathrm{d}(i_{\mathrm{D4}} - i_{\mathrm{D3}})}{\mathrm{d}t} + L_{34} \dfrac{\mathrm{d}i_{\mathrm{D4}}}{\mathrm{d}t} \right] \\ i_{\mathrm{D1}} - i_{\mathrm{D4}} = g_{\mathrm{fs}} \left[L_{\mathrm{b}} \dfrac{\mathrm{d}(i_{\mathrm{D4}} - i_{\mathrm{D1}})}{\mathrm{d}t} + L_{12} \dfrac{\mathrm{d}(i_{\mathrm{D2}} + i_{\mathrm{D3}} + i_{\mathrm{D4}})}{\mathrm{d}t} + L_{23} \dfrac{\mathrm{d}(i_{\mathrm{D3}} + i_{\mathrm{D4}})}{\mathrm{d}t} + L_{34} \dfrac{\mathrm{d}i_{\mathrm{D4}}}{\mathrm{d}t} \right] \end{cases} \tag{4.6}$$

In (4.6), it is obvious that the current imbalance between two MOSFETs is not only affected by the specific two MOSFETs drain currents, but also influenced by the other MOSFETs drain currents. For instance, the current imbalance between Q1 and Q4 is affected by all the four paralleled MOSFET currents. The phenomenon is named as the ‘current coupling effect’. Due to the current coupling effect, even though the two adjacent two MOSFETs has identical common source stray inductance mismatch, the current imbalances between the adjacent two MOSFETs are different. i_{D1} and i_{D2} have the largest different while i_{D3} and i_{D4} have the smallest imbalance.

To explain the current coupling effect influence on the current sharing performance, a generic DBC layout model is made as in Figure 4.3. This model has the same common source stray inductance mismatch with the

modeling in Figure 4.2, but the stray inductances are distributed in a different way without the current coupling effect. With Figure 4.3, the common source stray inductance for each SiC MOSFET is identical with that in Figure 4.2, which has been shown in (4.3). However, the voltages on the common stray inductances are different from that in (4.4), which are presented in (4.7).

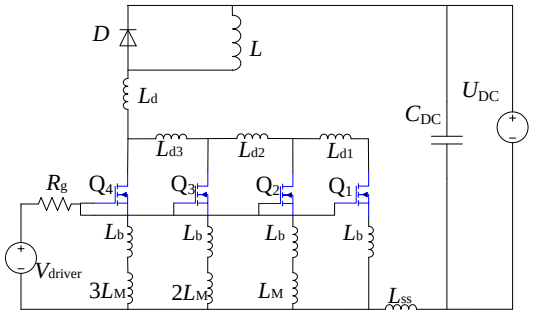


Figure 4.3 DBC layout modeling without current coupling effect

$$\begin{bmatrix} \triangle V_{\mathrm{LS1}} \\ \triangle V_{\mathrm{LS2}} \\ \triangle V_{\mathrm{LS3}} \\ \triangle V_{\mathrm{LS4}} \end{bmatrix} = \begin{bmatrix} L_{\mathrm{s1}} & L_{\mathrm{ss}} & L_{\mathrm{ss}} & L_{\mathrm{ss}} \\ L_{\mathrm{ss}} & L_{\mathrm{s2}} & L_{\mathrm{ss}} & L_{\mathrm{ss}} \\ L_{\mathrm{ss}} & L_{\mathrm{ss}} & L_{\mathrm{s3}} & L_{\mathrm{ss}} \\ L_{\mathrm{ss}} & L_{\mathrm{ss}} & L_{\mathrm{ss}} & L_{\mathrm{s4}} \end{bmatrix} \begin{bmatrix} i_{\mathrm{D1}} \\ i_{\mathrm{D2}} \\ i_{\mathrm{D3}} \\ i_{\mathrm{D4}} \end{bmatrix} \tag{4.7}$$

With (4.5) and (4.7), the current imbalance in the generic DBC layout with the identical common source stray inductance can be calculated as (4.8).

$$\begin{cases} i_{\mathrm{D1}} - i_{\mathrm{D2}} = g_{\mathrm{fs}}(\triangle V_{\mathrm{LS2}} - \triangle V_{\mathrm{LS1}}) = g_{\mathrm{fs}}\left[L_{\mathrm{b}} \dfrac{\mathrm{d}(i_{\mathrm{D2}} - i_{\mathrm{D1}})}{\mathrm{d}t} + L_{12} \dfrac{\mathrm{d}i_{\mathrm{D2}}}{\mathrm{d}t} \right] \\ i_{\mathrm{D2}} - i_{\mathrm{D3}} = g_{\mathrm{fs}}(\triangle V_{\mathrm{LS3}} - \triangle V_{\mathrm{LS2}}) = g_{\mathrm{fs}}\left[L_{\mathrm{b}} \dfrac{\mathrm{d}(i_{\mathrm{D3}} - i_{\mathrm{D2}})}{\mathrm{d}t} + L_{23} \dfrac{\mathrm{d}i_{\mathrm{D3}}}{\mathrm{d}t} \right] \\ i_{\mathrm{D3}} - i_{\mathrm{D4}} = g_{\mathrm{fs}}(\triangle V_{\mathrm{LS4}} - \triangle V_{\mathrm{LS3}}) = g_{\mathrm{fs}}\left[L_{\mathrm{b}} \dfrac{\mathrm{d}(i_{\mathrm{D4}} - i_{\mathrm{D3}})}{\mathrm{d}t} + L_{34} \dfrac{\mathrm{d}i_{\mathrm{D4}}}{\mathrm{d}t} \right] \\ i_{\mathrm{D1}} - i_{\mathrm{D4}} = g_{\mathrm{fs}}(\triangle V_{\mathrm{LS4}} - \triangle V_{\mathrm{LS1}}) = g_{\mathrm{fs}}\left[L_{\mathrm{b}} \dfrac{\mathrm{d}(i_{\mathrm{D4}} - i_{\mathrm{D1}})}{\mathrm{d}t} + (L_{12} + L_{23} + L_{34}) \dfrac{\mathrm{d}i_{\mathrm{D4}}}{\mathrm{d}t} \right] \end{cases} \tag{4.8}$$

With the comparison of (4.6) and (4.8), the current imbalance in the DBC layout of the power module is higher than the current imbalance in the generic DBC layout. The difference is due to the current coupling effect.

The mathematic analysis shows that the common source stray inductance mismatch can cause the current non-uniform distribution and the current coupling effect in this DBC layout aggravates the current imbalance. The essence of the current coupling effect is that the current densities (for L_1, L_2, L_3 and L_4) in the DBC segments are different, as shown in (4.6). The stray inductance affects the switching performance due to di/dt. In (4.6) even L_{12}=L_{23}=L_{34}, but the corresponding di/dt to them are different.

4.2 Ansys Q3D extraction of parasitic inductance in power module

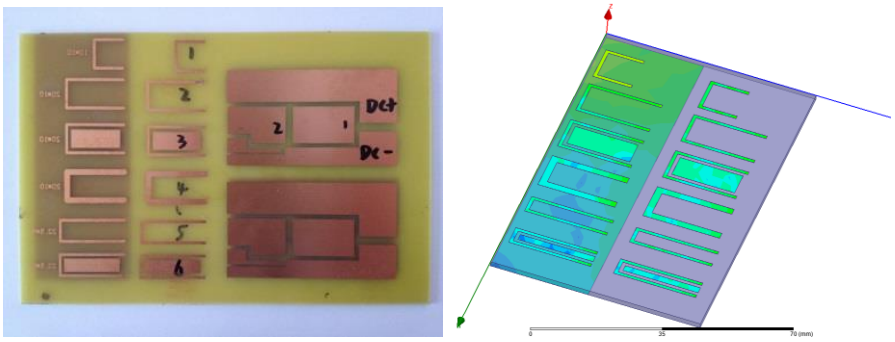
For the WBG device, the switching speed can be much higher than the Si devices. Consequently, the stray inductance will play a more important role in the switching performance of the WBG devices. In the power module, the stray inductance of the DBC traces and the bond wires should be better understood. In this research work, Ansys Q3D is employed for the extraction of the stray inductance of the DBC layout in the power module. The Q3D simulation results and the measurement results of the stray inductance are presented. An understanding of the Ansys Q3D modeling and the stray inductance extraction are the targets.

In many published research works [77, 78], Ansys Q3D was also used to extract the parasitic parameters in the power module. However, the extracted parasitic inductance is usually given as a specific number. In this chapter, a method of evaluating the Ansys Q3D simulation results is presented. With the evaluation method, the parasitic inductance in a power module with paralleled SiC MOSFET dies is extracted with Ansys Q3D. A better understand of the parasitic inductance is achieved and the extracted parasitic parameters are more trustable.

4.2.1 Ansys Q3D and impedance analyzer measurement

The main idea of evaluating the Ansys Q3D simulation is to make some simple traces both with the PCB circuit and the software Ansys Q3D. By comparing the measurement and the simulation results of the impedance of the simple traces, a better understand of the Ansys Q3D can be achieved.

Figure 4.4(a) shows a PCB board with some simple copper traces. Figure 4.4(b) shows the same geometry modeling in Ansys Q3D.



(a) (b)

Figure 4.4 PCB traces and its modeling with Ansys Q3D (a) PCB with copper traces (b) Ansys Q3D model

Several factors are considered in this evaluation process, including the trace length, the trace width, the trace covered area, with or without the bottom copper and the center filled copper. The detail information about the traces is shown in Table 4.1.

The impedance of the copper traces is measured with a precise impedance analyzer E4990A from Keysight, which has a bandwidth of 20Hz-120MHz. An example of the trace impedance is shown in Figure 4.5. The fitted curve is with the equivalent R-L series circuit. The Ansys Q3D simulation results with different frequencies and the measured results are shown in Table 4.2.

Table 4.1 PCB traces parameters

	L11	L12	L21	L22	L31	L32	L41	L42	L51	L52
Length(mm)	30	30	50	50	50	50	50	50	50	50
Area(mm2)	100	100	200	200	200	200	200	200	112.5	112.5
Width(mm)	1	1	1	1	1	1	2	2	1	1
Bottom cooper	Y	N	Y	N	Y	N	Y	N	Y	N
Center cooper	N	N	N	N	Y	Y	N	N	N	N

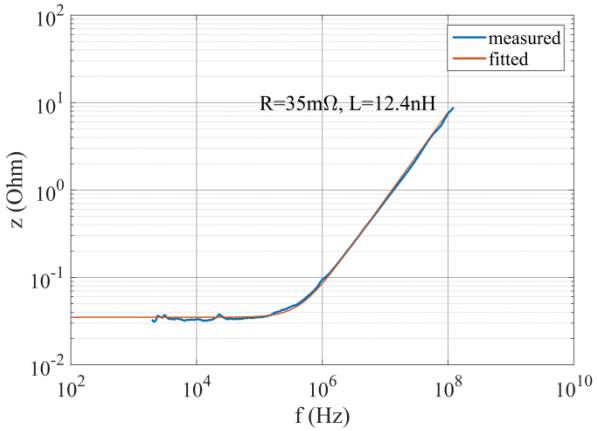


Figure 4.5 Measured and fitted impedance line with impedance analyzer

Table 4.2 PCB traces inductance simulation and measurement results

PCB traces inductance(nH)										
	L11	L12	L21	L22	L31	L32	L41	L42	L51	L52
DC	19.7	19.7	34.3	34.4	34.4	34.4	28.0	28.1	29.0	28.9
1MHz	16.6	19.7	28.1	34.4	27.3	32.2	20.8	27.9	25.6	29.1
30MHz	15.3	18.9	25.9	33.2	24.7	29.3	19.2	26.9	23.5	28.7
100MHz	15.2	18.8	25.7	33.0	24.4	29.0	19.0	26.7	23.3	28.1
Measured	12.4	15.9	21.5	29.7	20.0	26.1	16.3	24.1	21.4	27.9

With the results in Table 4.2, the simulation results and the measured results comparison is shown in Figure 4.6. The simulation results are with frequency 100MHz. The fitted line and the line equation are also presented in Figure 4.6. It can be observed that the simulation results and the measurement results have an approximate 4nH difference. One assumption of this 4nH offset is due to the short circuit calibration of the impedance analyzer probe. The probe is shown in Figure 4.7. The short circuit calibration tells the impedance analyzer that the impedance of this distance is zero. However, in the Ansys Q3D, all the traces are included in the calculation. Except the offset, the slope of the fitted line is very close to 1.

With the results in Table 4.2, some conclusion can be achieved. The bottom copper can reduce the inductance of the traces. The center copper can also reduce the inductance but the effect is not as big as the bottom copper.

Increasing the copper width can help reduce the trace inductance. With the same length, the covered area of the trace can also affect the inductance. The smaller covered area is, the smaller the trace inductance is.

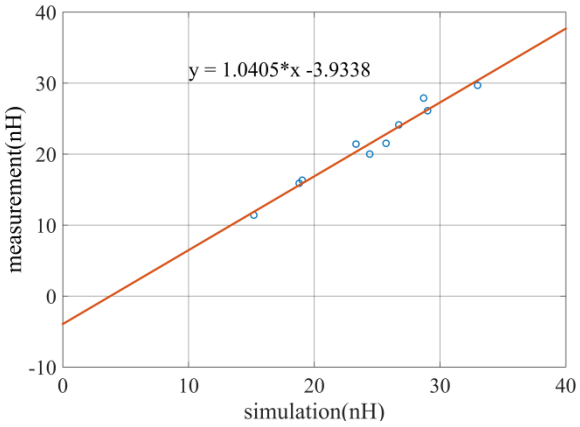


Figure 4.6 Simulation and measurement comparison

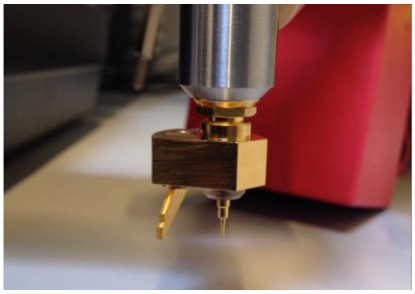


Fig 4.7 Impedance analyzer probe

4.2.2 Parasitic inductance extraction of the power module

The power module is shown in Figure 4.1(a) and its modeling is shown in Figure 4.8. The simulation is with two conditions. One condition is with the MOSFETs conducted and the other one is with the MOSFETs blocked. In Figure 4.9, the material of the MOSFET chips is copper while in Figure 4.10, the material of the MOSFET chips is silicon carbide. The simulation results with the current density are shown in Figure 4.9 and Figure 4.10. It is obvious that with the bottom copper, the current is more evenly distributed in the DBC traces. In Figure 4.9, the current densities in the DBC traces

segments are different, which validates the analysis of the current coupling effect.

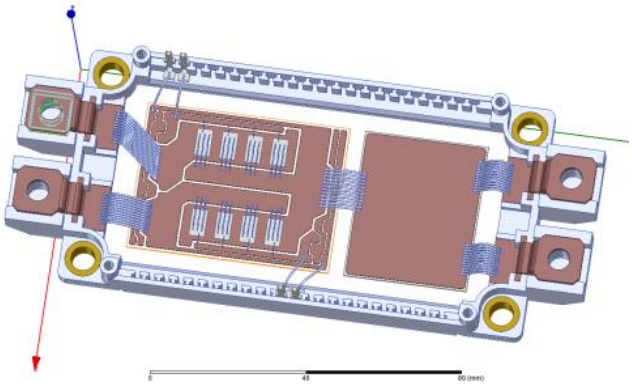
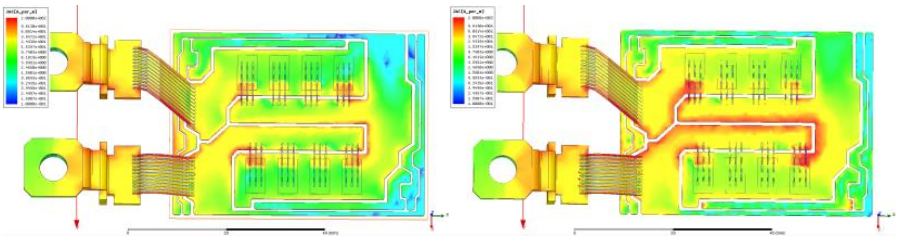
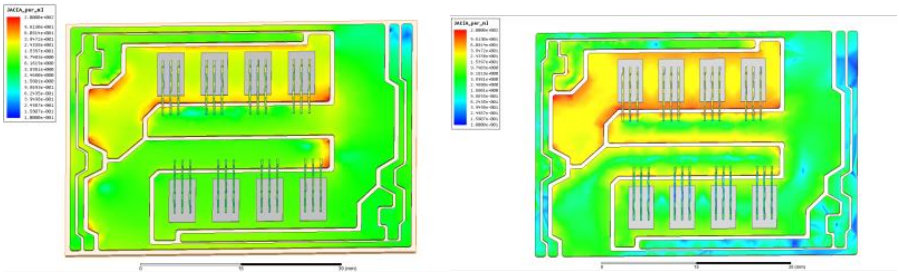


Figure 4.8 Power module model in Ansys Q3D



(a) (b)

Figure 4.9 Current density with MOSFETs conducted (a) with bottom copper (b) without bottom copper



(a) (b)

Figure 4.10 Current density with MOSFETs blocked (a) with bottom copper (b) without bottom copper

One example of the inductance curve is shown in Figure 4.11. It can be seen that the inductance decreases with the increase of the frequency. Above

1MHz, the inductance becomes more stable. The simulation results of the inductance at 10MHz are shown in Table 4.3.

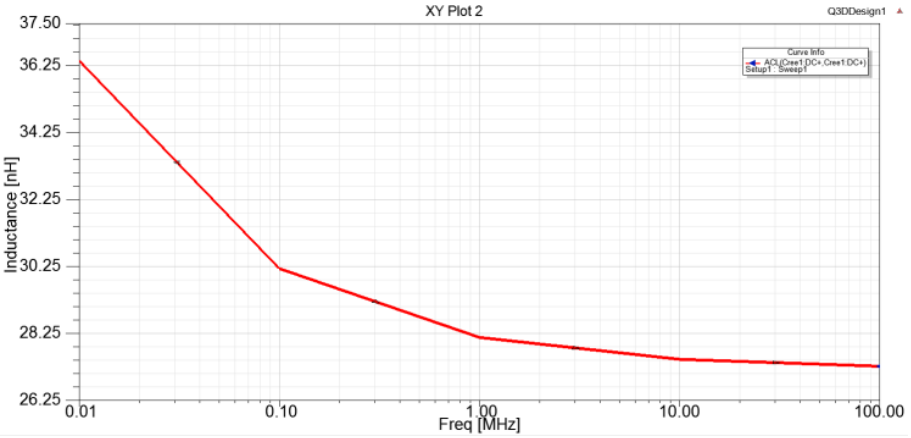


Figure 4.11 Inductance curve with different frequencies

Table 4.3 Simulation results

Bottom copper	With	Without
From screw terminal DC+ to DC-	27.39nH	38.12nH
Gate DBC traces with MOSFET blocked	16.40nH	19.82nH
DC+ DBC traces with MOSFET blocked	13.06nH	17.10nH
DC- DBC traces with MOSFET blocked	14.35nH	18.74nH
Single bond wire	5.73nH	

4.3 LTspice simulation study

According to the Ansys Q3D modeling and the measurement with impedance analyzer, the stray inductances are set as L_b=2nH, L_M=2nH and L_{ss}=5nH. With the parasitic inductances, the two circuit models presented in Figure 4.2 and Figure 4.3 are simulated with LTspice. The simulation results of these two circuits, with or without the current coupling effect, are shown in Figure 4.12 and Figure 4.13. The switching losses from the simulation are shown in Table 4.4.

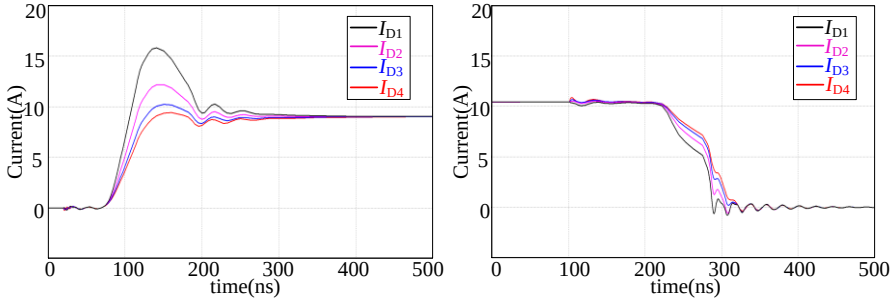


Figure 4.12 Simulation results with current coupling effect (R_g=10Ω)

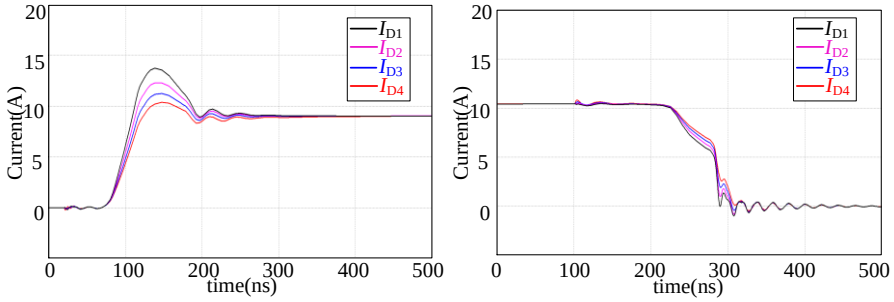


Figure 4.13 Simulation results without current coupling effect (R_g=10Ω)

With the comparison of Figure 4.12 and Figure 4.13, it is obvious that the current distribution with the current coupling effect is worse than that without the current coupling effect. The drain current waveform of Q_1 has a higher current overshoot with the current coupling effect in Figure 4.12. In Figure 4.12, the current differences between the nearby two MOSFETs are not identical while in Figure 4.13, the current differences between the nearby two MOSFETs are almost evenly distributed. This can also be explained with the mathematic analysis in (4.6) and (4.8).

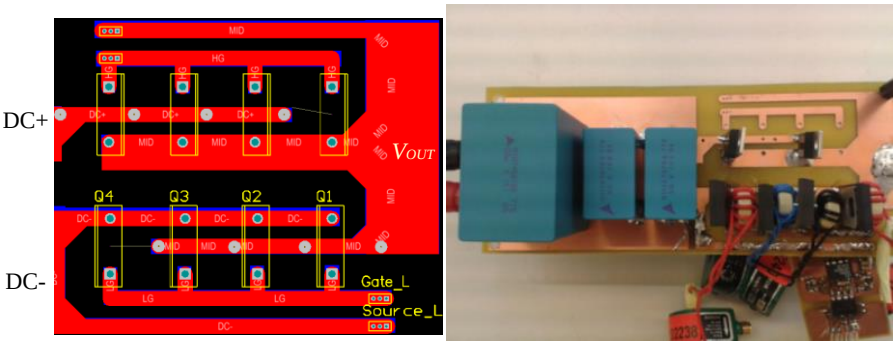
Table 4.4 Switching losses with and without the current coupling effect

current coupling effect	With				Without			
	Q_1	Q_2	Q_3	Q_4	Q_1	Q_2	Q_3	Q_4
Turn on loss (μJ)	428	330	273	246	410	367	332	304
Turn off loss (μJ)	145	180	213	234	128	142	157	172
Total loss (μJ)	573	510	486	480	538	509	489	476

The switching losses from the simulation results are presented in Table 4.4. For the switching loss difference caused by the current imbalance, the largest current mismatch is between Q_1 and Q_4. With the circuit mismatch and the current coupling effect, Q_1 and Q_4 have a 73.7% turn-on loss mismatch, 61.2% turn-off loss mismatch and 19.3% switching loss mismatch. Without the current coupling effect, Q_1 and Q_4 have a 35.0% turn-on loss mismatch, 34.3% turn-off loss mismatch and 13.1% switching loss mismatch.

4.4 Experimental study

At present, an accurate die current measurement in the power modules is not available. To experimentally evaluate the current sharing performance in the power module, a PCB circuit, which has the similar layout of the DBC of the SiC MOSFET power module, is designed. Figure 4.14(a) shows the PCB layout and Figure 4.14(b) shows the hardware prototype with the discrete packaged SiC MOSFETs (C2M0160120D).

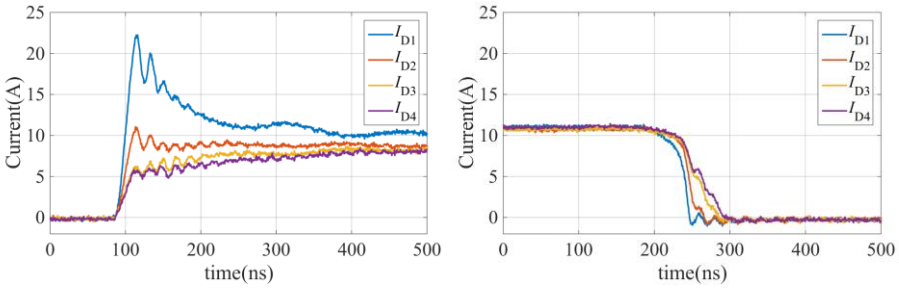


(a) (b)

Figure 4.14 PCB layout and double pulse test PCB circuit (a) PCB layout (b) PCB circuit hardware setup

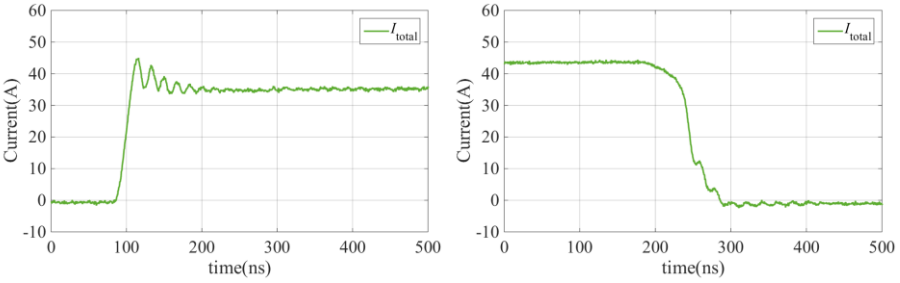
The DC-link voltage is 600V and the load inductor value is around 900μF. The four MOSFETs have a common gate resistor, which is 20Ω. The gate driver IC is IXDN614PI. The distance between the two adjacent SiC MOSFETs is around 14.5mm in the PCB circuit while in the DBC layout the distance is around 6mm. The current measurement of the SiC MOSFET drain current is by the two stage current measurement method with Pearson 2877. The experimental results with this PCB circuit are shown in Figure 4.15. Figure 4.16 shows the total switching current of the four paralleled

MOSFETs. With Figure 4.15 and Figure 4.16, it can be observed that even though the total power module current does not have a high overshoot and large oscillations, the individual transistors may exhibit large current overshoot due to the current imbalance.



(a) (b)

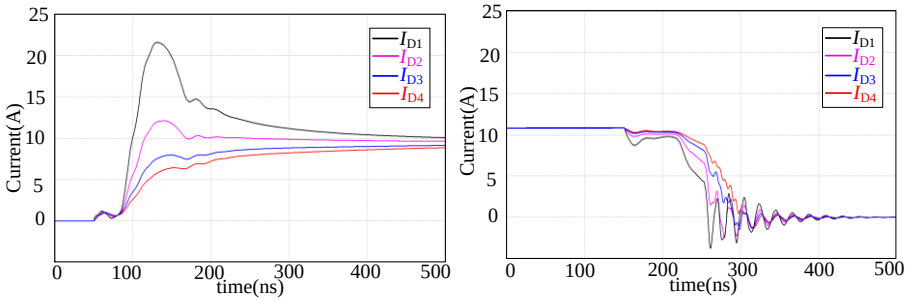
Figure 4.15 Experimental results of drain currents (a) turn on (b) turn off



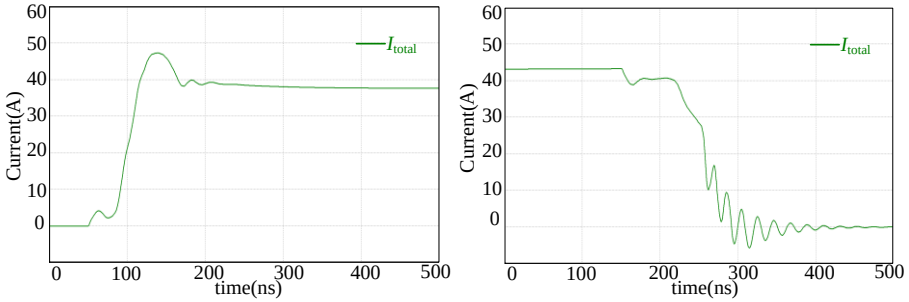
(a) (b)

Figure 4.16 Experimental results of total drain currents (a) turn on (b) turn off

The parasitic inductance of the PCB circuit is higher than that of the DBC layout. Therefore, the experimental results in Figure 4.15 have a larger current imbalance than the simulation results in Figure 4.12. If in the simulation circuit, the inductance of L_M is set to 6nH and the simulation switching speed is adjusted similar with the experimental one, the simulation results are shown in Figure 4.17. The Figure 4.17 simulation results match with the experimental results. With these experimental and simulation results, the influence of the common source stray inductance mismatch can be better understood.



(a)



(b)

Figure 4.17 Simulation results with L_M=6nH and R_g=5Ω (a) MOSFETs drain currents (b) total MOSFETs drain currents

4.5 DBC layout with auxiliary source bond wires

The auxiliary source bond wire for a single die is called Kelvin-Source connection. Infineon published the Cool MOS with the Kelvin-Source connection, as show in Figure 4.18[62]. The Kelvin-Source connection decouples the gate-source loop and the drain source loop. Therefore, the Kelvin-Source connection can avoid the common source stray inductance effect, improve the switching speed and reduce the switching losses.

Figure 4.18 TO247 packaged MOSFET with and without Kelvin-Source connection

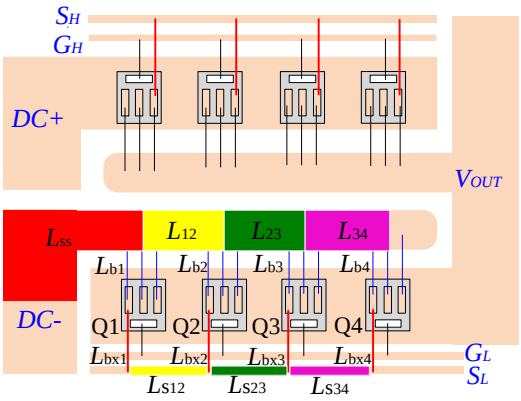


Figure 4.19 DBC layout with auxiliary source bond wires

In the power modules with paralleled dies, the auxiliary source bond wires are also widely used. One DBC layout for the power module with the auxiliary source bond wires is show in Figure 4.19. Compared with the DBC layout in Figure 4.1, the DBC layout in Figure 4.19 has the auxiliary source bond wires for each die. This section discusses the working mechanism of the auxiliary source bond wires, including the benefits with the auxiliary bond wires and the current distribution in the power module with the auxiliary source bond wires. The auxiliary source connections are analyzed in two periods. One is the MOSFETs on-state period and the other one is the switching transient period. In the MOSFETs on-state period, the auxiliary source connections are considered as inductors while during the MOSFETs switching transient period, the auxiliary source connections are considered as resistors.

4.5.1 Current imbalance mitigation with auxiliary source bond wires

For the transient current distribution, the model of the DBC layout in Figure 4.19 is shown as Figure 4.20. One benefit of the auxiliary source connections is that the common source stray inductance of the power module is reduced by decoupling L_{ss}. Another merit of the auxiliary source connections is that the current imbalance among the paralleled MOSFETs can be mitigated.

To analyze the model in Figure 4.20 and the current distribution in the power module with the auxiliary source bond-wire, it is reasonable to simplify the

model to paralleling two SiC MOSFETs, as shown in Figure 4.21. Figure 4.21(a) shows the model of paralleling two SiC MOSFETs without the auxiliary source bond-wire. Figure 4.21(b) shows the model of paralleling two SiC MOSFETs with the auxiliary source bond-wire.

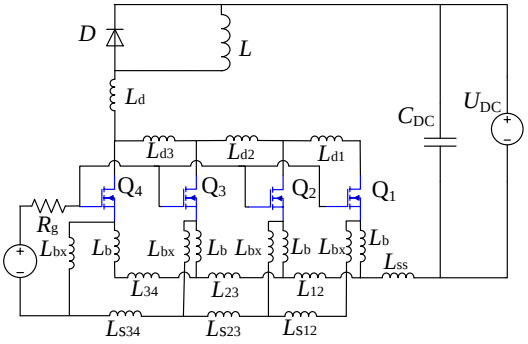
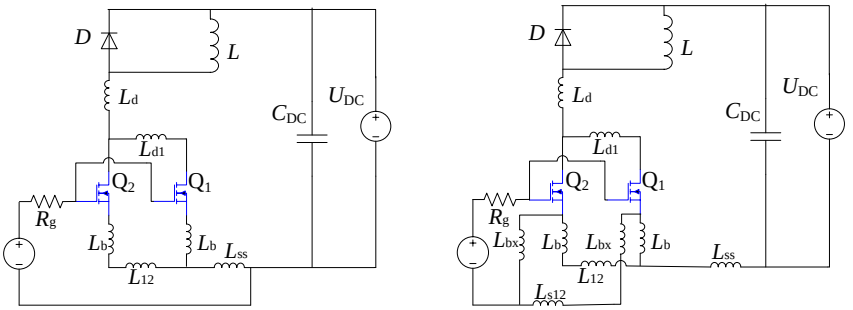


Figure 4.20 DBC layout modeling with the auxiliary source bond wires



(a) (b)

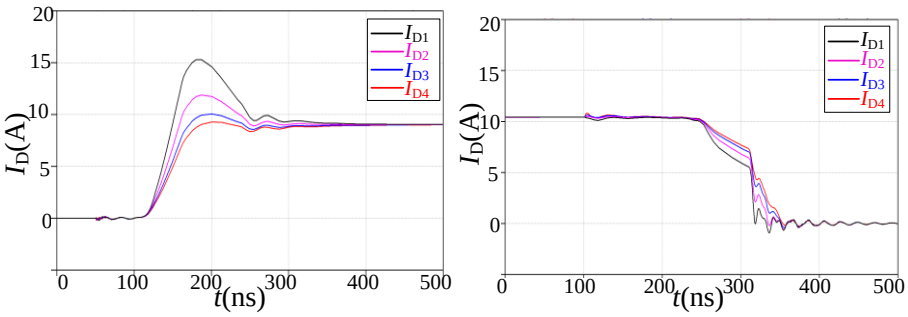
Figure 4.21 Two SiC MOSFETs in parallel (a) without auxiliary source connection (b) with auxiliary source connection

With the similar analysis of (4.6) and (4.8), the current imbalance of the paralleled two SiC MOSFETs in Figure 4.21(a) and Figure 4.21(b) can be described as (4.13) and (4.14), respectively.

$$i_{\mathrm{D1}} - i_{\mathrm{D2}} = g_{\mathrm{fs}}[(L_{\mathrm{b}} + L_{12})\frac{\mathrm{d}i_{\mathrm{D2}}}{\mathrm{d}t} - L_{\mathrm{b}}\frac{\mathrm{d}i_{\mathrm{D1}}}{\mathrm{d}t}] \tag{4.13}$$

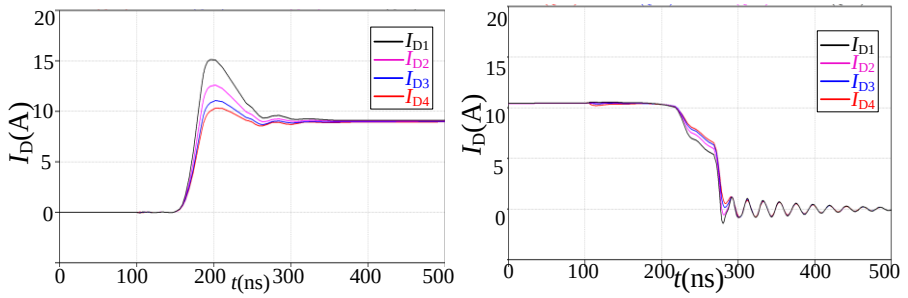
$$i_{\mathrm{D1}} - i_{\mathrm{D2}} = g_{\mathrm{fs}}\frac{2L_{\mathrm{bx}} + L_{\mathrm{s12}}}{2L_{\mathrm{b}} + L_{12} + 2L_{\mathrm{bx}} + L_{\mathrm{s12}}}[(L_{\mathrm{b}} + L_{12})\frac{\mathrm{d}i_{\mathrm{D2}}}{\mathrm{d}t} - L_{\mathrm{b}}\frac{\mathrm{d}i_{\mathrm{D1}}}{\mathrm{d}t}] \tag{4.14}$$

With (4.13) and (4.14), it is obvious that with the same current switching speed, the current imbalance of the paralleled two SiC MOSFETs with the auxiliary source bond wire is reduced as the factor of $k=(2L_{bx}+L_{s12})/(2L_{bx}+L_{s12}+2L_b+L_{12})$, which is always smaller than 1. But the stray inductance of the auxiliary source connection $(2L_{bx}+L_{s12})$ is usually a few times larger than the stray inductance of the source power loop $(2L_b+L_{12})$. Therefore, the current imbalance mitigation effect of the auxiliary source bond wires is limited.



(a) (b)

Figure 4.22 Current sharing performance without the auxiliary source connection (R_g=10Ω, t_r=60ns) (a) turn on (b) turn off

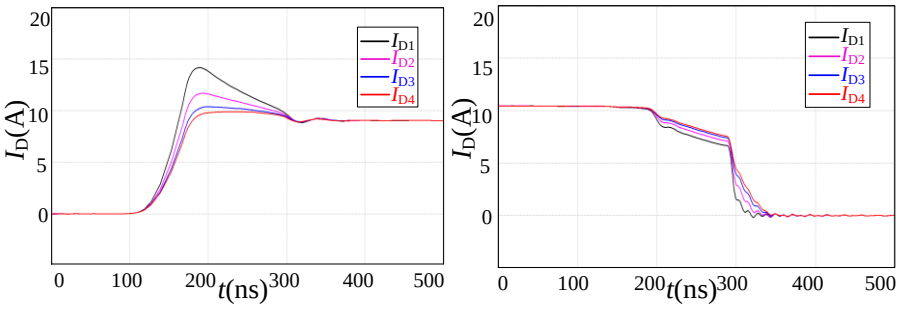


(a) (b)

Figure 4.23 Current sharing performance with the auxiliary source connection (R_g=10Ω, t_r=30ns) (a) turn on (b) turn off

In the LTspice simulation, the stray inductances are set as $L_b=L_M$=2nH and $L_{bx}=L_{sx}$=6nH. The simulation results of model with the auxiliary source bond-wires are shown in Figure 4.22 and Figure 4.23. Compared Figure 4.22 and Figure 4.23, with the auxiliary source bond-wire, the four paralleled

MOSFETs turn on and turn off faster. This validates that the auxiliary source bond wires can reduce the common source stray inductance and improves the switching speed of the power module. From the current sharing point of view, the current imbalance among the paralleled dies is also smaller with the auxiliary source bond wires, even though the switching speed is increased. This validates that with the auxiliary source bond wires, the current imbalance among the paralleled die can be mitigated.



(a) (b)

Figure 4.24 Current sharing performance with auxiliary source connection (R_g=23Ω, t_r=60ns) (a) turn on (b) turn off

The experimental results with the auxiliary source connections are presented in Figure 4.25. The auxiliary source connections are introduced with wires. The experimental results in Figure 4.25 have a smaller current imbalance than the results in Figure 4.15 and the current switching delay among the paralleled dies are also reduced dramatically. However, the total current has a larger switching oscillations and overshoot compared with the experimental results in Figure 4.16. This is because that the total common stray inductance is reduced with the auxiliary source connections. Therefore, the switching speed of the 'power module' is increased with the same gate resistance. The faster switching speed causes larger oscillations and overshoots. From the experimental results of the power module current with and without auxiliary source bond wires, the power module current with the auxiliary source bond wires is 'worse' than the one without the auxiliary source bond wires. However, the individual current of each MOSFET is 'better' than the one without the auxiliary source bond wires. It states that a nice power module total current cannot indicate that the die current in the

power module also behaves nicely. The current distribution in the power module with paralleled dies has to be analyzed according to the DBC layout.

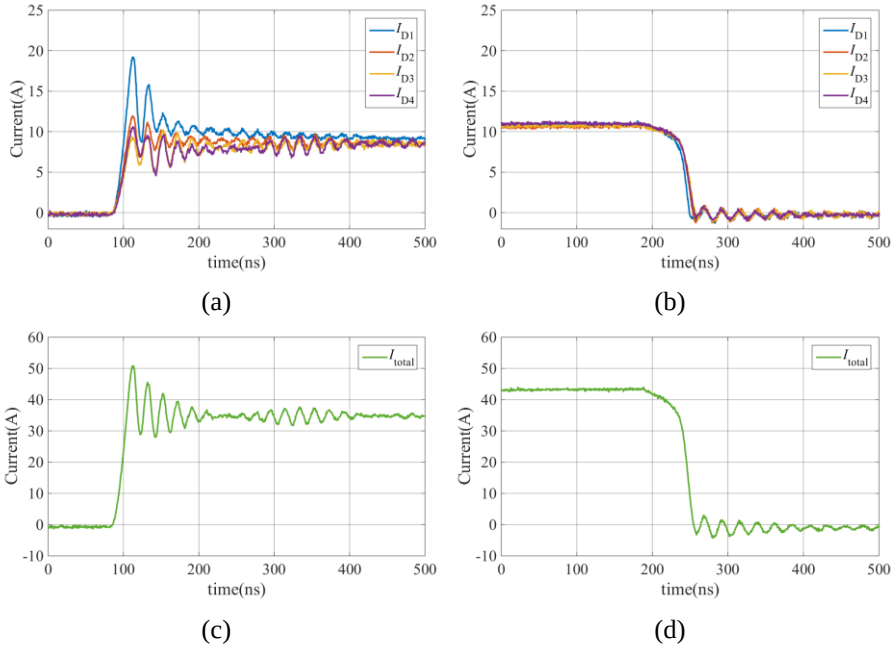


Figure 4.25 Experiment results with the auxiliary source connection (a) turn on (b) turn off (c) total current turn on (d) total current turn off

4.5.2 Current stress on the auxiliary source bond wires

The Kelvin-Source connection only takes the gate loop current and there is no coupling effect between the Kelvin-Source connection and the power current loop. However, in the power module with paralleled dies, the auxiliary bond wires are still in the power current loop. For instance, in Figure 4.19 the MOSFET drain current I_{D4} can go to the DC- terminal by L_b-L_{34}-L_{23}-L_{12}-L_{ss}, which is the expected path. But it can also go through L_{b4}-L_{s34}-L_{s23}-L_{s12}-L_{b1}-L_b-L_{ss}, even though this current loop has higher impedance than the expected one.

To mathematically analyze the current distribution in the DBC layout with the auxiliary source bond wires, both during on state period and switching transient, the model of the DBC layout with four SiC MOSFETs in parallel is shown in Figure 4.26(a). During on state period, the bond wires and the

DBC traces are not only considered as inductors but summarized as impedance which includes both the resistance and the inductance.

Similarly, if two SiC MOSFETs are paralleled, as shown in Figure 4.18(b), the current distribution in the bond wires can be mathematically calculated with the impedance of the current loops. I_{Zbx2} can be calculated as (4.9). The current of Z_{bx1} has the identical amplitude of I_{Zbx2}, but the opposite current direction. $Z_{b1}=Z_{b2}=Z_b$, $Z_{bx1}=Z_{bx2}=Z_{bx}$. Gate driver current is overlooked in this analysis since there is no gate current except the switching transient and the gate current in the during the switching transient is very small compared with the power current.

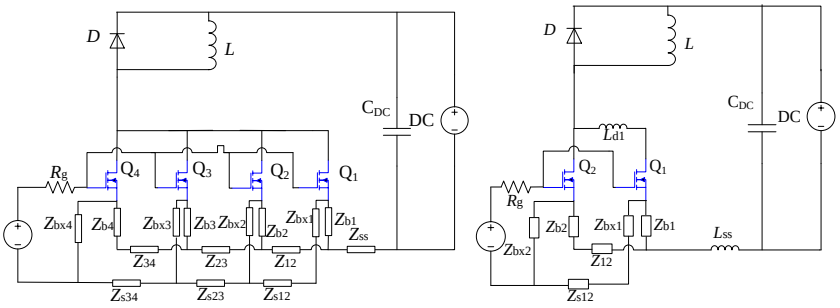


Figure 4.26 Model with the impedance of the auxiliary source bond wires (a) four MOSFETs in parallel (b) two MOSFETs in parallel

$$I_{Zbx2}=\frac{(I_{D2}-I_{D1})Z_b}{2(Z_b+Z_{bx})+(Z_{12}+Z_{s12})}+\frac{I_{D2}Z_{12}}{2(Z_b+Z_{bx})+(Z_{12}+Z_{s12})} \tag{4.9}$$

$$I_{Zbx2}\approx I_{D2}\frac{Z_{12}}{2(Z_b+Z_{bx})+(Z_{12}+Z_{s12})}=I_{D2}(P+j\omega Q) \tag{4.10}$$

$$P=\frac{R_{12}(2R_b+2R_{bx}+R_{12}+R_{s12})+\omega^2L_{12}(2L_b+2L_{bx}+L_{12}+L_{s12})}{(2R_b+2R_{bx}+R_{12}+R_{s12})^2+\omega^2(2L_b+2L_{bx}+L_{12}+L_{s12})^2} \tag{4.11}$$

$$Q=\frac{L_{12}(2R_b+2R_{bx}+R_{s12})-R_{12}(2L_b+2L_{bx}+L_{s12})}{(2R_b+2R_{bx}+R_{12}+R_{s12})^2+\omega^2(2L_b+2L_{bx}+L_{12}+L_{s12})^2} \tag{4.12}$$

With (4.9), the current of the auxiliary source bond wires depends on the mismatch of the drain currents, the drain currents and impedance of the bond wires and the DBC traces. The mismatch of I_{D1} and I_{D2} are assumed very

small compared with the drain currents. If the impedance Z is replaced with $Z=R+j\omega L$, I_{Zbx2} can be presented with (4.10)-(4.12).

In the DBC layout of paralleling four SiC MOSFETs, the current distribution in the auxiliary source bond wires can also be mathematically calculated, but it will be difficult to analyze as there are too many impedance loops. However, the conclusion from the analysis with two paralleled dies can be extended to four paralleled dies.

If it is assumed that the resistance of the auxiliary source bond wires and traces is three times of the resistance of the power bond wires and traces, i.e. $Z_{b4}=Z_{34}=Z_{b3}=Z_{23}=Z_{b2}=Z_{12}=Z_{b1}=Z$, $Z_{bx4}=Z_{s34}=Z_{bx3}=Z_{s23}=Z_{bx2}=Z_{s12}=Z_{bx1}=3Z$, as shown in Figure 4.27. The MOSFET drain currents are I_D. The current distribution of the auxiliary source bond wires in the power module can be calculated as (4.13). The currents of the power source bond wires are, therefore, calculated as in (4.14).

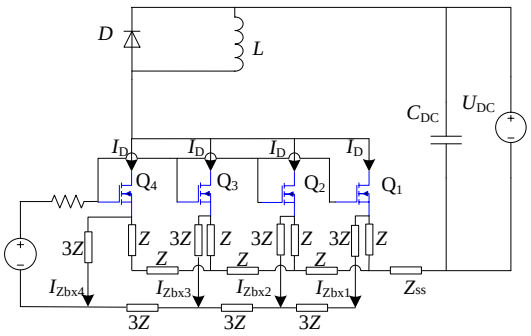
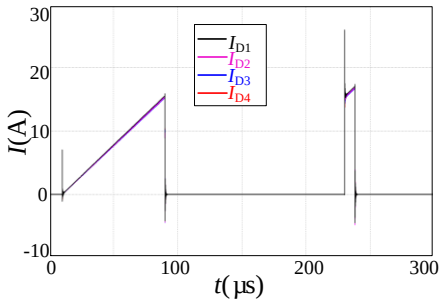


Figure 4.27 An example model with specific impedance definition

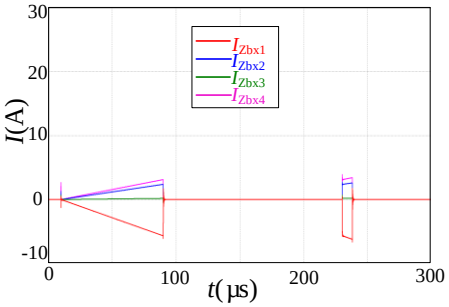
From (4.13), the auxiliary source bond wires of Q_1 are under the highest current stress. And the current direction of I_{Zbx1} is opposite with the expected direction, which increases the current of the power source bond wires of Q_1. From (4.14), the source bond wires of Q_1 are under a higher pressure than the other source bond wires and the current stress on the source bond wires of Q_1 is almost 1.5 times of the designed value of the drain current. If $Z=R+j\omega L$, R=0.5mΩ and L=2nH, the corresponding simulation results are shown in Figure 4.28.

$$\begin{cases} I_{Zbx1} = -\dfrac{31}{84} I_D \\ I_{Zbx2} = \dfrac{1}{84} I_D \\ I_{Zbx3} = \dfrac{13}{84} I_D \\ I_{Zbx4} = \dfrac{17}{84} I_D \end{cases} \tag{4.13}$$

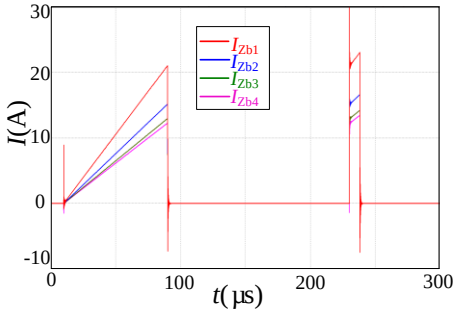
$$\begin{cases} I_{Zb1} = \dfrac{115}{84} I_D \\ I_{Zb2} = \dfrac{83}{84} I_D \\ I_{Zb3} = \dfrac{71}{84} I_D \\ I_{Zb4} = \dfrac{67}{84} I_D \end{cases} \tag{4.14}$$



(a)



(b)



(c)

Figure 4.28 Simulation results with the auxiliary source bond wires

For this power module, the parameters of the bond wires and the DBC traces are shown in Table 4.5. The parameters are calculated or estimated according to the geometry and the material properties of the bond wires and the DBC traces. With the parameters in Table 4.5, the current distribution in the auxiliary source bond wires and the SiC MOSFETs in the power module are simulated with LTspice. The simulation results are shown in Figure 4.29.

Table 4.5 Parameters of bond wires and DBC traces

	Resistance (mΩ)	Inductance (nH)
Source bond wires	1.62/3	6/3
Auxiliary source bond wire	1.62	6
DBC trace between two dies	0.126	2
Auxiliary trace between two dies	0.504	6

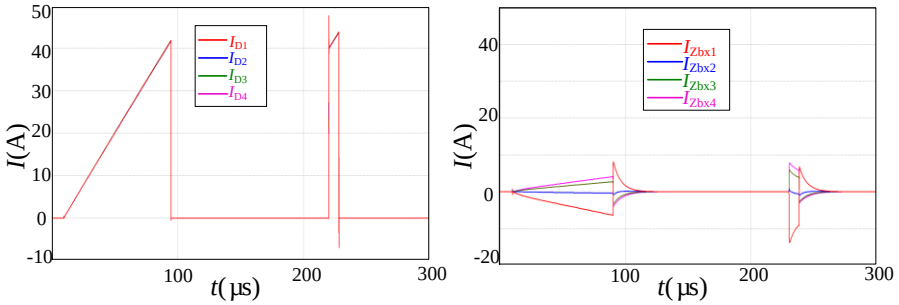


Figure 4.29 Simulation results of the MOSFET drain currents (I_{D1}-I_{D4}) and currents of the auxiliary source bond wires (I_{Zb1}-I_{Zb4})

The current for each SiC MOSFET die is around 40A while the current in the auxiliary source bond wire can be up to 10A. In this simulation condition, the auxiliary source bond wire current capability is 1/3 of the power bond wires. Even though, the current stress on the auxiliary source bond wire is not beyond the current capability, the large current on the auxiliary source bond wires are not expected. The high current of the auxiliary source bond wires may cause extra oscillations among the paralleled source pads of the dies, which affects the switching behavior of the device.

With the PCB circuit and the discrete SiC MOSFETs, the experimental results are shown in Figure 4.30. The simulation results are different from

the experimental results, because the current rating and the circuit parameters in the DBC circuit and the PCB circuit are different.

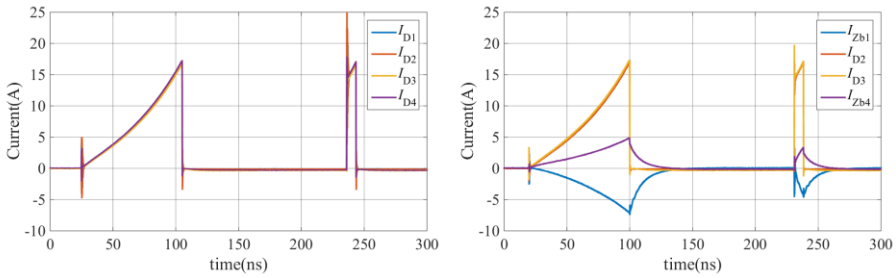


Figure 4.30 Experimental results of the MOSFET drain currents (I_{D1}-I_{D4}) and currents of the auxiliary source connections (I_{Zb1}-I_{Zb4})

Usually the auxiliary source connections are designed to decouple the gate current and the power loop current and they are not expected to carry the power current. However, in the power module with this DBC layout in Figure 4.19, the auxiliary source bond wires are still in the power current loop. Moreover, there may be extra oscillations among the source pads of the paralleled dies. Therefore, an external source resistor can be used to introduce into the auxiliary source bond wires to suppress the power current and to damping the possible oscillations.

4.5.3 Essence of the transient current imbalance

With the auxiliary source bond wires, the current imbalance can be reduced, however, not eliminated. According to the modeling and the analysis of the two DBC layouts, the essence of the transient current imbalance can be summarized as below.

The mismatch of the common source stray inductance causes the mismatch of the gate source voltages during the switching transient. The transient mismatch of the gate source voltages leads to the switching current imbalance among the paralleled dies. Therefore, in one power module with paralleled dies, to evaluate the transient current distribution, the direct way is to investigate the mismatch of the gate source voltages. As the paralleled dies usually work with a common gate driver, the mismatch of the gate source voltage is the voltage potential difference between the source pads of the paralleled MOSFET dies. For example, the transient current mismatch

between Q_3 and Q_4 are determined by the voltage difference of u_{GS4} and u_{GS3}, which is the voltage potential difference between the two points S_3 and S_4, i.e. u_{S3S4}, as shown in Figure 4.31.

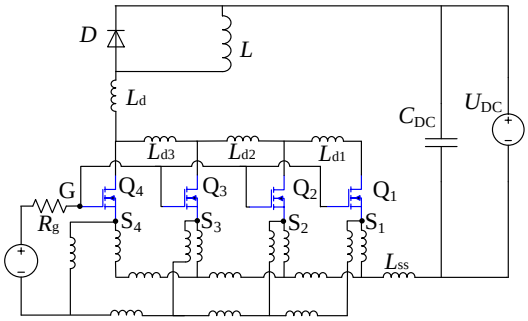


Figure 4.31 Model with the source pads indicated

The auxiliary source connections are in parallel with the power source traces, thereby reducing the total stray inductance for the power current. With the same d*i*/dt, the voltage potential difference between the source points is also reduced. Consequently, the transient current imbalance is mitigated. On the other hand, this is also why the auxiliary source connections are also under the stress of the power current. The more current goes through the auxiliary source connections, the more mitigation effect the auxiliary source connections brings. Consequently, the higher current stresses on the auxiliary source connections are. In this way, the essence of the transient current imbalance and the circuit mismatch is the voltage potential difference between the difference source terminals. No matter with or without the auxiliary source bond wires, as long as the power current follows the designed traces, there are always voltage potential differences at the difference source terminals in this DBC layout pattern.

4.6 Conclusion

This chapter studies the circuit mismatch and the current coupling effect influence on the current distribution in the power modules with parallel connection of SiC MOSFETs. According to the analysis and experimental results, it shows that the circuit mismatch in the power module causes the current imbalance among the paralleled dies in the power module while the current coupling worsens the current distribution. With the new findings of

the circuit mismatch and the current coupling effect in the power module with paralleled dies, the transient current imbalance in the power modules with similar DBC layouts are mathematically understood and explained. This knowledge shows that the common source stray inductance is a critical parasitic parameter for the current sharing performance of the paralleled dies in the power module. Therefore, for the future DBC layout design of the power modules with paralleled dies, an important guideline for a better transient current distribution of the paralleled dies can be concluded: reducing the mismatch of the common source stray inductance can mitigate the transient current imbalance. Besides the circuit mismatch and the current coupling effect, this chapter also investigates the effects of the auxiliary source bond connections in the power module with paralleled dies. The auxiliary source bond wires can mitigate the current imbalance among the paralleled dies and they can also reduce the total common source stray inductance. However, it has to be aware that the auxiliary source bond wires in the power module with paralleled dies works in the different way from the Kelvin-Source-Connection. The current stress on the auxiliary source bond wires needs to be paid attention. To reduce the current stress on the auxiliary source bond wires, a separate source resistor can be introduced in the power module.

5 Split output DBC layout for SiC MOSFET multichip power modules

In chapter 4, the current distribution in the power module with the paralleled SiC MOSFETs dies is mathematically analyzed and experimental investigated regarding the circuit mismatch in the power module. The non-uniform transient current distribution in the conventional DBC layout is observed. This chapter proposes a novel DBC layout for the power module with paralleled power semiconductors.

There are two merits of the proposed DBC layout for the power module with paralleled power semiconductors. One merit is that the proposed DBC layout optimizes the current sharing performance among the paralleled dies in the power module. The other merit is that the DBC layout is with the split output topology, which can decouple the junction capacitance and the body diode of the SiC MOSFET in a bridge configuration. Consequently, the split output topology can achieve a reduced switching loss in the circuit with bridge configurations.

In this chapter, the split output topology in a half bridge configuration is first presented. The current commutation mechanism of the half bridge with split output is described step by step. An efficiency comparison between the traditional half bridge and the half bridge with split output is presented. Successively, a half bridge DBC layout with split output is proposed for the power module with paralleled SiC MOSFETs. The DBC layout is presented and modeled regarding the parasitic inductance of the bond wires and DBC traces. The simulation and experimental results show that the current distribution performance in the proposed DBC layout is improved by reducing the circuit mismatch among the paralleled dies.

5.1 Split output half bridge

SiC MOSFET has an intrinsic body diode, which has a relatively high forward voltage drop and reverse recovery phenomenon. The high forward voltage drop could cause high conduction losses in the condition that the

body diode works as a freewheeling diode. The reverse recovery current could cause extra switching losses. Consequently, in a bridge configuration, the usage of SiC MOSFET body diode is not recommended and an external anti-paralleled Schottky diode is suggested by the manufacture [26]. However, the external anti-paralleled diode increases the total junction capacitance, which also makes a contribution to the switching losses, especially for high switching frequency applications. Moreover, in the medium voltage range, the conduction of the SiC MOSFET body diode is not recommended due to the reliability issues.

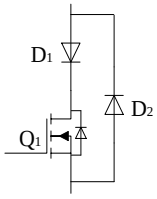


Figure 5.1 Two external diode solution to blocking body diode

To avoid the body diode conducting current, the traditional solution is to put a diode in series with the SiC MOSFET and then parallel another external diode, as shown in Figure 5.1 [26]. Using this method, two external diodes are required, which increases the semiconductor area, the device cost and the complexity of the system. Especially for the power module, the DBC area is larger with two external diodes and the layout design freedom is also limited. To fully utilize the fast switching capability of SiC MOSFETs and avoid the limitations of SiC MOSFET body diode in the bridge configuration, a split output topology was proposed[42, 43]. A half bridge with split output is depicted in Figure 5.2. The split output of a half bridge can be achieved with a coupling inductor, as an example of Figure 5.2(a). The equivalent circuit can be with three separate inductors, as an example of Figure 5.2(b). L_{f1} and L_{f2} are the effective leakage inductance of L_1 and L_2. The analysis and experimental validation of half bridge can be applied in many other converters and inverters. Therefore, the analysis and experimental study is with half bridge shown in Figure 5.2(b).

The salient merit of the split output configuration is that it decouples both the MOSFET body diode and the junction capacitance, which means that in the split output half bridge these two SiC MOSFETs do not see each other

directly. Besides that, the circuit design has more freedom compared to the traditional half bridge. The top SiC MOSFET and bottom one are not necessarily placed very close to minimize the stray inductance. The circuit stray inductance between these two switches is part of the leakage inductance which is needed in this topology. At present, however, there is no current commutation mechanism and experimental efficiency analysis in these existing literatures. Before split output is applied in SiC MOSFET inverters and more application fields, a fully understanding of split output is required. Therefore, there is a need to make the current commutation mechanism and experimental efficiency analysis and validation.

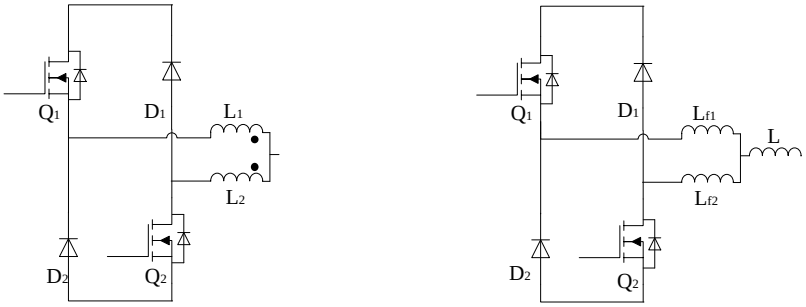


Figure 5.2 A half bridge with split output (a) with coupling inductor (b) with separate inductors

5.1.1 Current commutation mechanism of split output half bridge

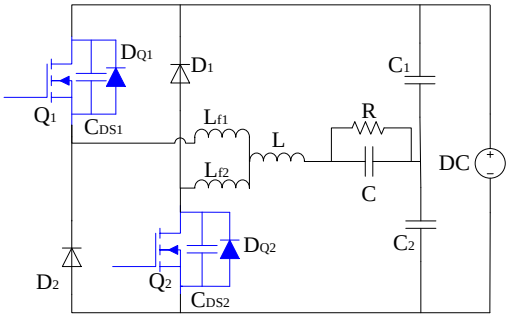


Figure 5.3 Half bridge inverter with split output

The half bridge split output current commutation mechanism is analyzed with the half bridge working as an inverter, as shown in Figure 5.3. A typical control signal with the dead time of the SiC MOSFETs Q_1 and Q_2 is shown in Figure 5.4. S_1=1 S_2=1 means that Q_1 and Q_2 are closed while S_1=0 S_2=0 means Q_1 and Q_2 are open.

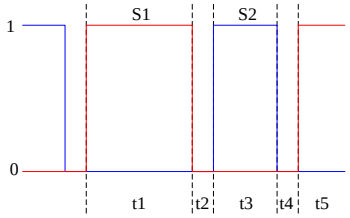


Figure 5.4 Typical control signal

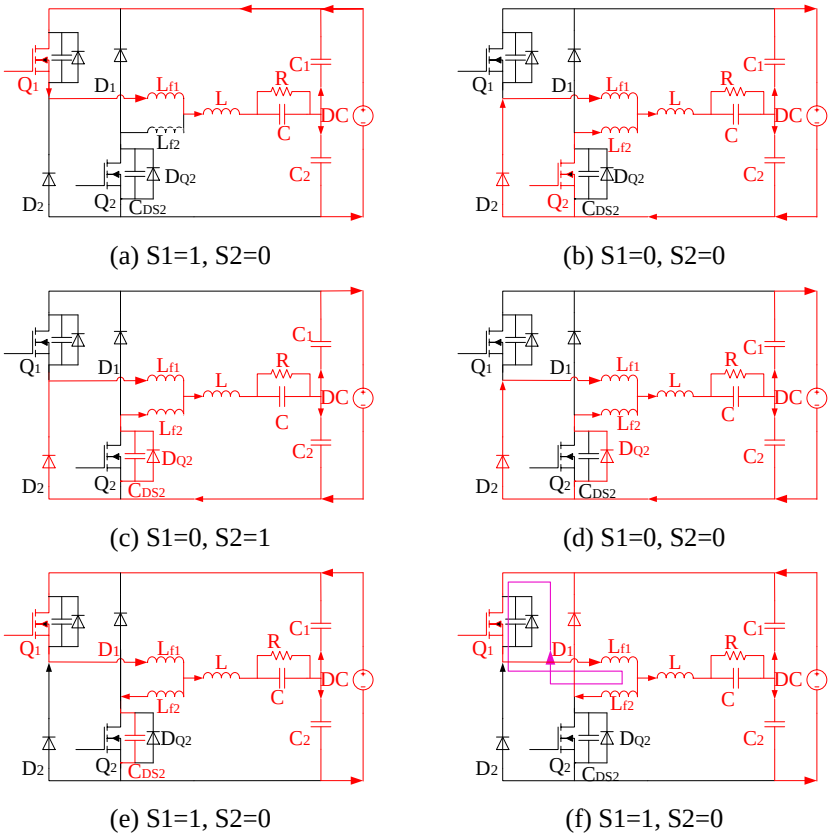
In a half bridge inverter, the working conditions are divided into two cases in terms of different directions of the load inductor current (i_L). One condition is that the direction of i_L is from left to right. The other condition is that the direction of i_L is from right to left. Under the first condition, the current commutation processes (red color) are divided into 6 steps, shown in Figure 5.5(a) to Figure 5.5(f).

The first step is shown in Figure 5.5(a), which is in t1 period (S_1=1, S_2=0) in Figure 5.4. The load current commutates through Q_1, L_{f1}, L and R, C, and then goes back to the DC capacitors and the DC power supply. The currents of L_{f1} and L are identical i_{Lf1}=i_L.

The second step is shown in Figure 5.5(b), which is in t2 period (S_1=0, S_2=0) in Figure 5.4. Q_1 turns off. The inductor L_{f1} has a tendency of keeping the current i_{Lf1}. Consequently, D_2 turns on as a freewheeling diode. C_{DS2} is the junction capacitance of the SiC MOSFETs Q_2. Before Q_1 turns off, u_{CDS2}=U_{DC}. In the second step in Figure 5.5(b), C_{DS2} discharges to $u_{CDS2} \approx 0$ through L_{f2}. Therefore, there is a current in L_{f2} as in Figure 5.5(b). After C_{DS2} is fully discharged, i_{Lf2} commutates to the body diode of the SiC MOSFET Q_2. Compared with i_{Lf1}, i_{Lf2} is much smaller as i_{Lf2} is the freewheeling current of the discharge of the junction capacitance.

The third step is shown in Figure 5.5(c), which is in t3 time period (S_1=0, S_2=1) in Figure 5.4. Q_2 turns on and the channel of the SiC MOSFET Q_2 is

reverse conducted. i_{Lf2} starts to commutate through Q_2. In this time period, i_{Lf2} is still quite small, as the voltage applied on L_{f2} and Q_2 is negligible.



(a) S1=1, S2=0

(b) S1=0, S2=0

(c) S1=0, S2=1

(d) S1=0, S2=0

(e) S1=1, S2=0

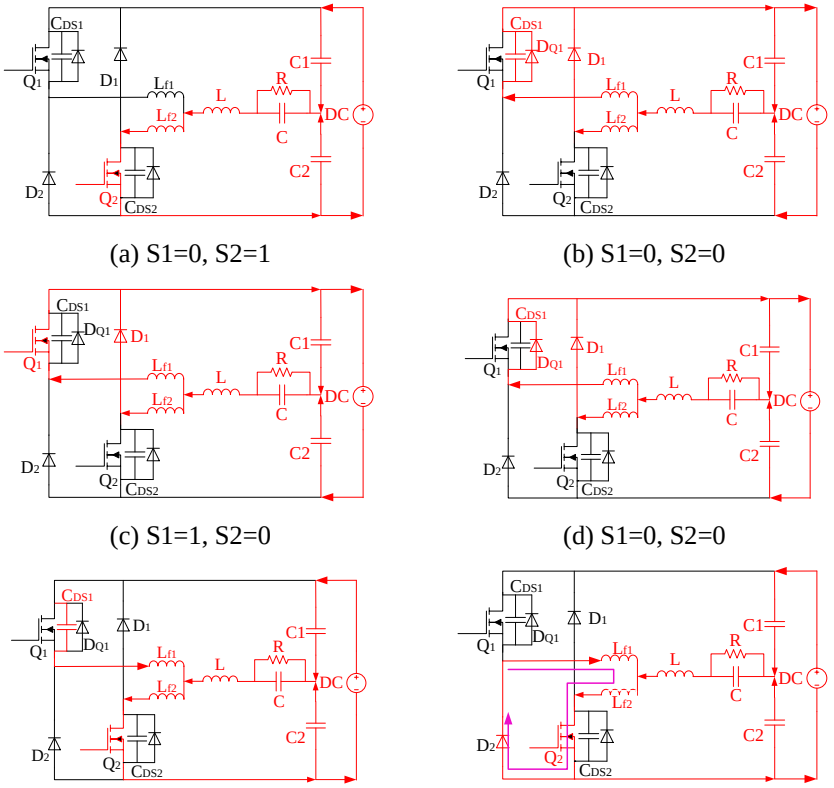
(f) S1=1, S2=0

Figure 5.5 Current commutation processes with positive load inductor current

The fourth step is presented in Figure 5.5(d), which is in t4 time period (S_1=0, S_2=0) in Figure 5.4. Q_2 turns off. i_{Lf2} commutates through the body diode D_{Q2} again, as shown in Figure 5.5(d). Figure 5.5(b)-(d) shows that the split output topology decouples the body diode of SiC MOSFET in bridge configurations.

The next two steps are the transient between t4 and t5 in Figure 5.4. The two steps are shown in Figure 5.5(e) and Figure 5.5(f). In the beginning of t5 time period S_1=1, S_2=0, Q_1 turns on and Q_2 turns off. C_{DS2} needs to be charged to $u_{CDS2}=U_{DC}$ by i_{Lf2} as shown in Figure 5.5(e). After C_{DS2} is fully charged, i_{Lf2} still exists and commutates to D_1, then goes back through Q_1 and L_{f1}, as presented in Figure 5.5(f). After i_{Lf2} decreases to zero, the current

commutation process is as that in Figure 5.5(a) again. The two steps in Figure 5.5(e) and Figure 5.5(f) demonstrate how the split output topology decouples the junction capacitance of the SiC MOSFET. In Figure 5.5(e) and Figure 5.5(f), the charging current of C_{DS2} cannot directly add to the current of Q_1. It has to go through L_{f2} and L_{f1}. L_{f1} and L_{f2} store the energy of the charging current and release the energy later. While in the traditional half bridge, the charging current of one MOSFET junction capacitance causes a current overshoot in the other MOSFET. The current overshoot leads to extra switching losses. Therefore, in the half bridge with split output, the switching loss is smaller than that in the traditional half bridge.



(a) S1=0, S2=1

(b) S1=0, S2=0

(c) S1=1, S2=0

(d) S1=0, S2=0

(e) S1=0, S2=1

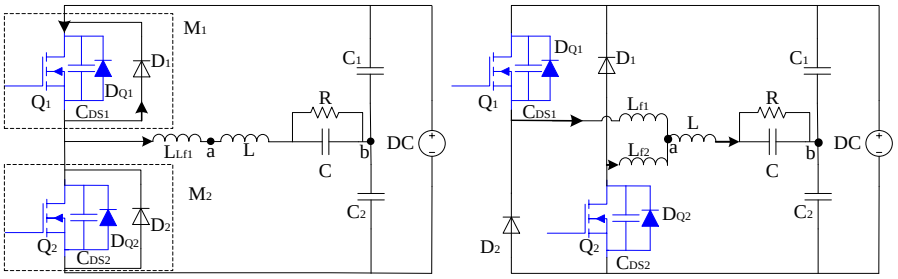
(f) S1=0, S2=1

Figure 5.6 Current commutation processes with negative load inductor current

The other condition is that the direction of i_L is from right to left. In this condition, the analysis is similar with the first condition and not repeated. The current commutation processes are presented in Figure 5.6.

5.1.2 Comparison between traditional and split output half bridge

Two half bridge circuits with SiC MOSFETs are shown in Figure 5.7. One is the traditional half bridge with external paralleled schottky diode and the other one is the half bridge with split output. These two half bridge circuits are simulated in LTspice. The LTspice models of the SiC MOSFETs are from Cree. In this simulation, U_{DC}=600V. L=5mH. L_{f1}=L_{f2}=50 μH. R=20Ω. C=10 μF. The positive current directions of the devices and the inductors in the simulation results are defined as in Figure 5.7. The half bridge inverters works with the same SPWM modulation method, which has a switching frequency of 20 kHz.



(a) (b)

Figure 5.7 half bridge circuits (a) traditional half bridge (b) split output half bridge

The simulation results of the load inductor currents are shown in Figure 5.8. There is little difference between the load inductor currents of these two half bridges. It indicates that the split output does not change the output current performance.

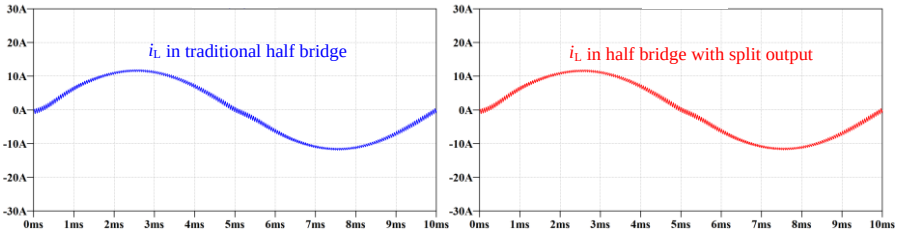


Figure 5.8 Load inductor currents comparison

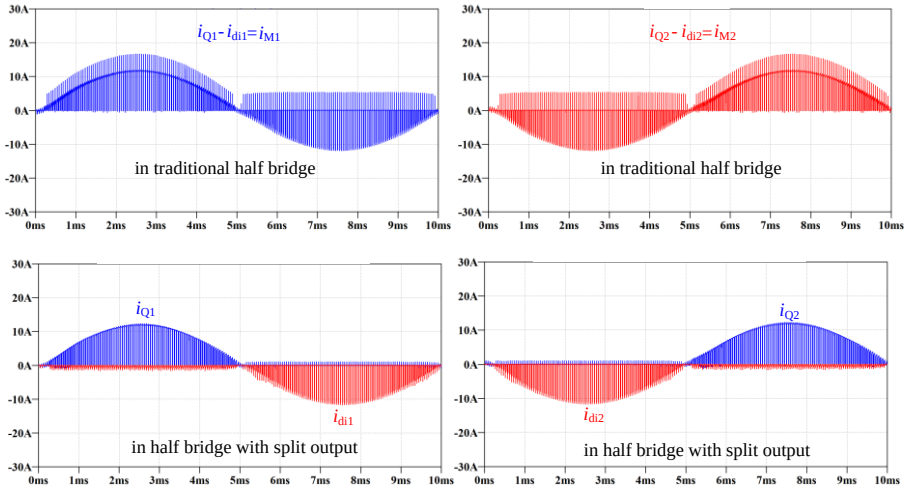
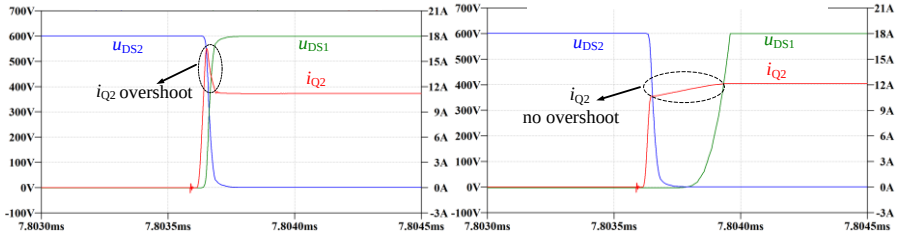


Figure 5.9 Device currents of the simulation results

In the traditional half bridge, the SiC MOSFETs and the paralleled external schottky diodes are considered as combined switches Q_1 and Q_2, as shown in Figure 5.7. The current of Q_1 and Q_2 affects the switching losses. The currents of the SiC MOSFETs and the schottky diodes in these two half bridge circuits are shown in Figure 5.9.

Compared with the SiC MOSFET and diode currents in the traditional half bridge, the SiC MOSFETs in the half bridge with split output have much smaller current overshoots and spikes. Take a turn-on example of Q_2, the simulation results are shown in Figure 5.10. In the traditional half bridge, when Q_2 turns on, there is an overshoot current of i_{Q2}, which is caused by the capacitive charge of C_{DS1} and the reverse recovery current during the switching transient. The current overshoot of i_{Q2} leads to extra switching losses as the current overshoot exists before u_{DS2} falls down. In the half bridge with split output, however, there is no current overshoot of i_{Q2}. The capacitive charge of C_{DS1} in the half bridge with split output still exists. But the charging current cannot directly add to i_{Q2} due to the inductors L_{f1} and L_{f2}. There is no overshoot of i_{Q2}. In this way, the charging current of C_{DS1} causes little extra switching losses in Q_2. The energy from the charging current is stored in L_{f1} and L_{f2} during the switching transient. In Figure 5.10(b), there is a time period that both u_{DS2} and u_{DS1} are zero. In this period, L_{f1} and L_{f2} hold

the DC link voltage and keep the energy. After that, L_{f1} and L_{f2} release the energy to the load inductor.

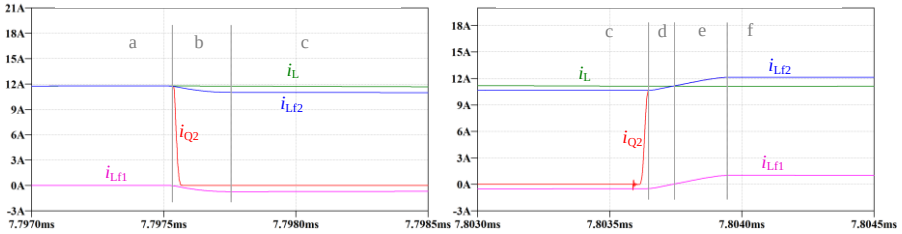


(a) (b)

Figure 5.10 Device currents comparison (a) in tradition half bridge (b) in half bridge with split output

The specific turn-on of Q_2 in Figure 5.10(b) and the previous one turn-off processes of Q_2 are shown in Figure 5.11 with the inductors currents. The current commutation processes are indicated as 'a' to 'f' according to Figure 5.6(a) to Figure 5.6(f). The simulation results in Figure 5.10 and Figure 5.11 validate that the split output topology decouples the junction capacitance and the body diode of the SiC MOSFET in the bridge configurations. Consequently, the half bridge with split output has smaller switching losses compared with the traditional half bridge counterpart in the same condition.

The forward voltage drop of the SiC Schottky diode is smaller than that of the SiC MOSFET body diode in the same breakdown voltage level. Therefore, the conduction loss of Schottky diode is smaller than that of the body diode of SiC MOSFET with the same forward current amplitude. In the applications where the body diode works as a freewheeling diode, both switching loss and conduction loss can be reduced in the bridge configuration with split output. But in the half bridge inverter, the conduction loss may not be reduced. Because dead time is very short, when the SiC MOSFET works in the reverse conduction mode, the conduction loss of SiC MOSFET may be smaller than the Schottky diode if $R_{on} \times I_Q < V_F$ ($I_F = I_Q$). R_{on} is the on resistance of SiC MOSFET. I_Q is the current through the MOSFET. V_F is diode forward voltage drop.



(a) (b)

Figure 5.11 Simulation results of the current commutation process (a) Q_2 turn off (b) Q_2 turn on

5.1.3 Leakage inductance and device current

The simulation study shows that the split output topology can decouple the junction capacitance and the reverse recovery effect of the body diode. In the simulation study, the leakage inductance of L_{f1} and L_{f2} are 50 μH, which is 1% of the load inductance 5mH. In this section, the influence of the leakage inductance is studied based on LTspice simulation.

The LTspice simulation results are shown in Figure 5.12. In Figure 5.12(a), the leakage inductance varies from 1nH to 100 μH while the total load inductance keeps as 1mH. With the increase of the leakage inductance, the MOSFET turn-on current overshoot decreases. The leakage inductance has little influence on the drain-source voltages. In Figure 5.12(b), the total load inductance is adjusted to 5mH and the leakage inductance keeps the same sweep. The MOSFET current in Figure 5.12(b) has a small difference with that in Figure 5.12(a). In Figure 5.12(c), the DC link voltage is adjusted from 600V to 300V. The current overshoot is reduced as the capacitive charge becomes smaller. Besides that, the MOSFET turn-on current keeps the similar trend with that in Figure 5.12(a). In Figure 5.12(d), the total load inductance is set as 60 μH. The simulation results are presented with different leakage inductance.

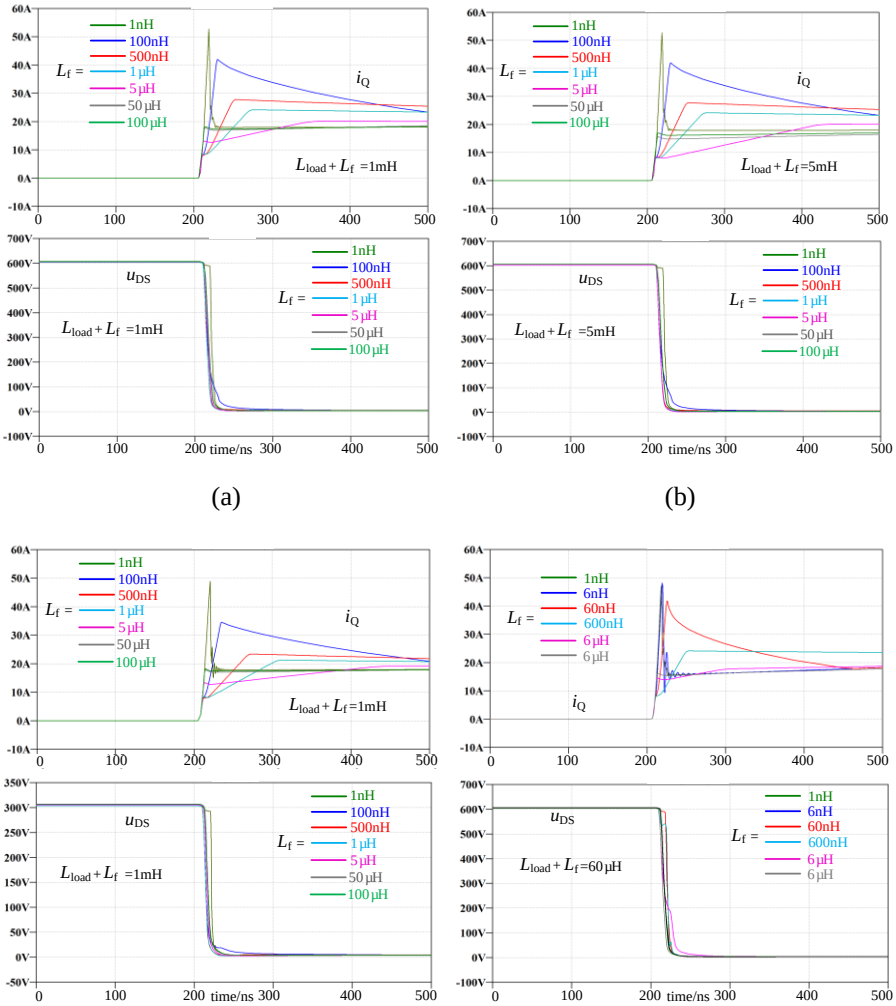


Figure 5.12 LTspice simulation results with different leakage inductance

From the simulation results, it can be concluded that the leakage inductance has an obvious effect on the MOSFET turn-on current while it has little effect on the MOSFET turn-on drain source voltage. With Figure 5.12(d), if the leakage inductance is 6nH, the MOSFET turn on current overshoot is even larger than with 1nH. It means that the leakage inductance is not always reducing the device current overshoot. If the MOSFET current overshoot needs to be optimized, the leakage inductance should be selected carefully.

5.1.4 Experimental results

To verify the analysis of the half bridge with split output, hardware setup circuits are designed with SiC MOSFET (C2M0080120) and SiC Schottky (C4D20120) diode from Cree. The hardware circuits are double pulse test circuits and the half bridge power circuits. The double pulse test circuit can show the current commutation process in the switching transient. Simultaneously, the SiC MOSFETs and Schottky diode current of the double pulse test circuits can be measured with high bandwidth current measurement methods. With the device currents, the current commutation process can be validated. The half bridge power circuits are used to make the efficiency comparison between the half bridge with split output and the traditional half bridge. The validity of experiment study largely depends on the accuracy of the measurement system, especially for the device current measurement. The measurement equipment is shown in Table 1.

Table 1. Measurement equipment

Part No.	Description	Bandwidth	Mesured signal
DL9040	Oscilloscope	500MHz	
Pearson 2877	Current Monitor	200MHz	i_{di}, i_Q
Passive probe	Voltage probe	400MHz	u_{DS}

Two circuits of half bridge hardware setups are designed. One is the traditional half bridge with external paralleled Shottky diode, as shown in Figure 5.13(a) and the other one is the half bridge with split output as shown in Figure 5.13(b). The switching losses comparison is between Q_2 in the half bridge with split output and Q_4 in the traditional half bridge. The hardware setup of the double pulse test circuit with split output is shown in Figure 5.13(c). Gate drivers of Q_2 and Q_4 have the identical gate resistance. The DC link voltage is 600V.

The experiment results of double pulse test circuits are shown in Figure 5.14. Figure 5.14(a) shows the switching waveforms and the switching loss of Q_2. Figure 5.14(b) shows switching waveforms and the switching losses of Q_4. Even though an external Schottky diode D_3 is paralleled with Q_3, a larger overshoot of Q_4 current is still observed in Figure 5.14(a) compared with the current overshoot of Q_2 in Figure 5.14(b). The larger current overshoot of Q_4

is caused by the charging current of the junction capacitance of Q_3 and D_3. As shown in Figure 5.14(a), the turn-on switching loss of Q_4 is 480μJ while turn-on switching loss of Q_2 is only 350μJ. Q_4 has around 37% larger turn-on loss than that of Q_2 due to its larger current overshoot. Q_4 and Q_2 have very similar turn-off loss, as shown in Figure 5.14(a) and Figure 5.14(b). It indicates that by decoupling the body diode and the junction capacitance of the SiC MOSFET, the switching loss of SiC MOSFET in a bridge configuration with the split output topology can be reduced.

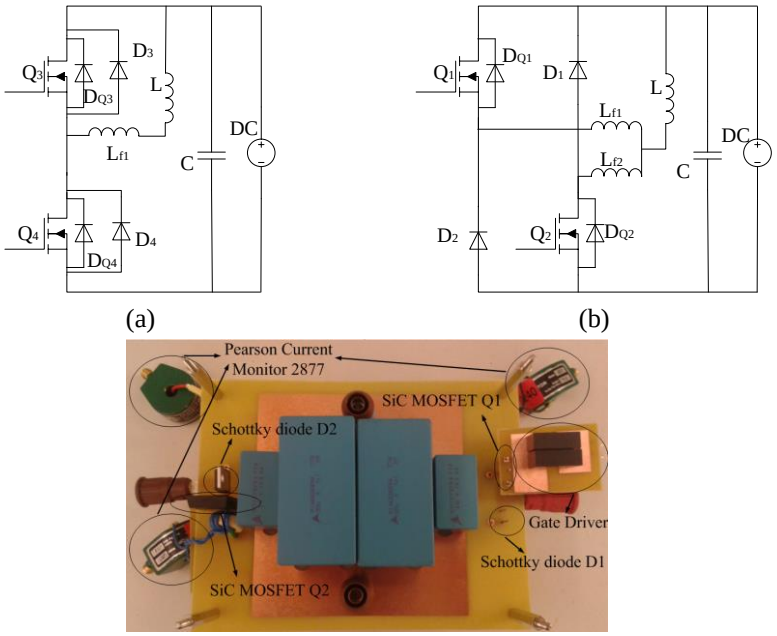
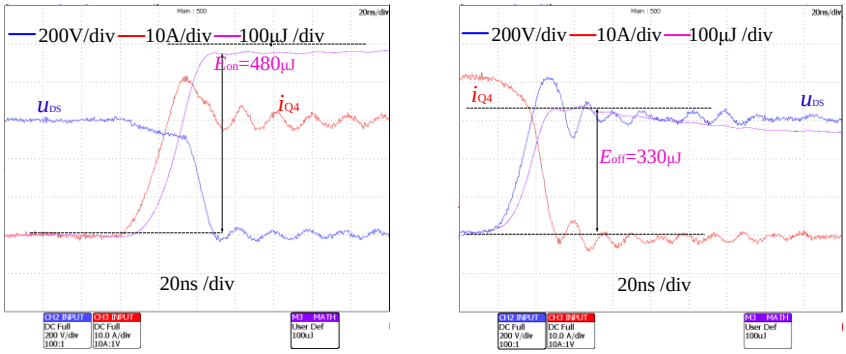
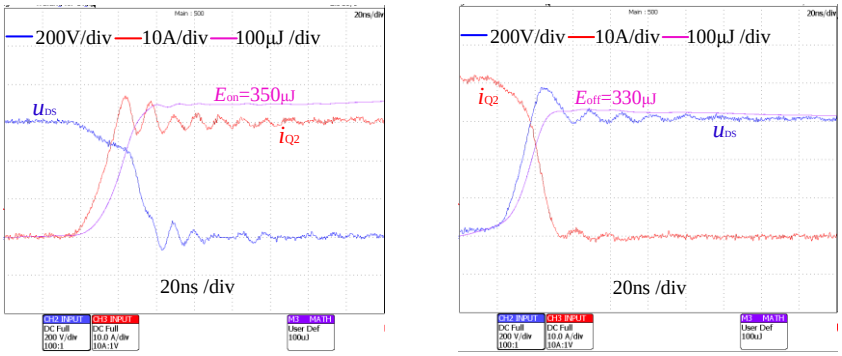


Figure 5.13 Double pulse test circuit schematic and hardware setup (a) traditional half bridge (b) split output half bridge (c) hardware setup of split output double pulse test circuit

Figure 5.15 shows the device current of Q_1, D_1 and Q_2 in double pulse test. Figure 5.15(b) shows the detail commutation process when Q_2 turns off. After Q_2 turns off, i_{Q1} is only around 1A while i_{D2} is more than 30A. It indicates that most of load current i_L commutates into D_2. As the forward voltage drop of D_2 is smaller than that of D_{Q1}, in a condition that the body diode works as freewheeling diode, the converter may have a smaller diode conduction loss with split output.

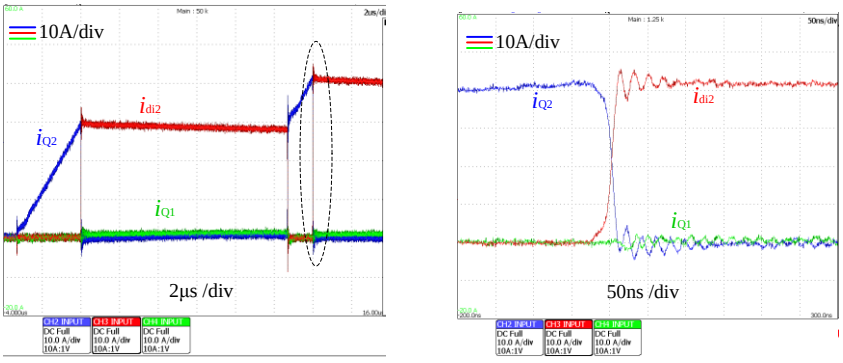


(a)



(b)

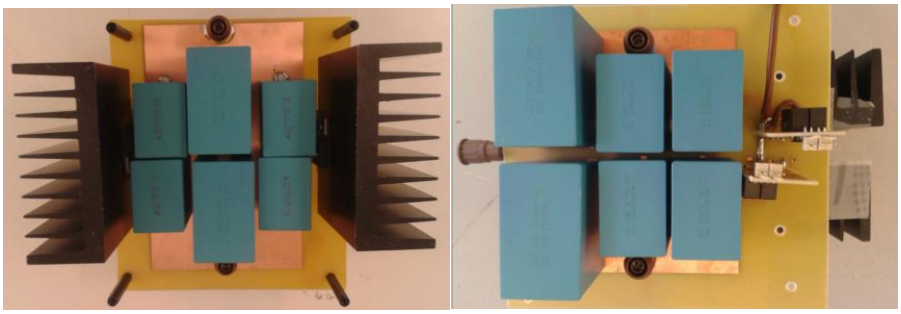
Figure 5.14 Switching losses comparison (a) Switching transient of SiC MOSFET Q_4 in the traditional half bridge (b) Switching transient of SiC MOSFET Q_2 in split output half bridge



(a) (b)

Figure 5.15 Current commutation processes of split output half bridge

Besides the double pulse test circuit experimental study, two half bridge circuits as shown in Figure 5.16 are designed to test the output and the efficiency analysis of the split output half bridge circuit. Figure 5.16(a) shows the split output half bridge inverter hardware setup. Figure 5.16(b) shows the traditional half bridge inverter hardware setup. As seen in Figure 5.16(a), in the half bridge with split output, there is no need to place the top SiC MOSFETs and bottom SiC MOSFET very close as what it should be in the traditional half bridge. The stray inductance between the two SiC MOSFETs is not as critical as in the traditional half bridge. More feasible layout design is another merit with the split output, especially for the DBC layout design of the power modules.



(a) (b)

Figure 5.16 Half bridge power inverter with split output (a) half bridge inverter with split output (b) traditional half bridge inverter

The experimental conditions for these two half bridge circuits are similar. The load inductance is around 900 μH. The inductance of L_{f1} and L_{f2} is around 30 μH. The inductors are made with three separate magnetic cores. The DC link voltage is 600V. The SiC MOSFETs in the experimental study have the same type of gate drivers and the two circuits have the same type of heat sinks. The two half bridge circuits work with the same SPWM modulation method. Figure 5.17 shows an example of the output current i_R of the half bridge with split output.

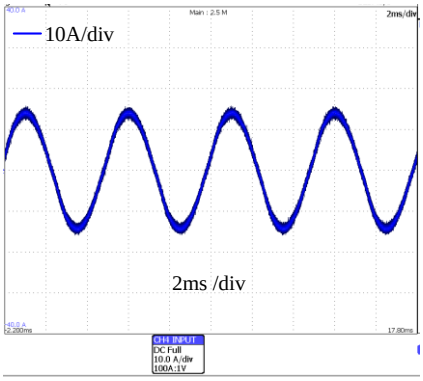


Figure 5.17 Output current of half bridge with split output

Figure 5.18 shows the efficiency comparison with different switching frequencies from 10 kHz to 100 kHz. The load current is adjusted from 3A to 20A by changing the load resistance R in Figure 5.7. The efficiencies of these two half bridge inverters are measured with a precision power analyzer PPA5530 from Newtons4th Ltd. The output power is measured between points 'a' and 'b', as shown in Figure 5.7. To make a fair comparison, L_{f1} is put in series with the load inductor L in the traditional half bridge.

The traditional half bridge has a higher efficiency at 10 kHz, which can be explained with that the conduction loss of Schottky diode may be higher than that of SiC MOSFET working in synchronous mode. However, when the switching frequency is larger than 25 kHz, the half bridge with split output has a higher efficiency than the traditional half bridge. With the increase of the switching frequency, the efficiency improvement of the half bridge with split output also increases. At 50 kHz, the peak efficiency difference between the traditional half bridge and the half bridge with split output is around 0.31%. While at 100 kHz, the peak efficiency with split output is improved by 0.5%. It implies that the half bridge with split output has a lower switching losses and the topology with split output is suitable for the high switching frequency applications.

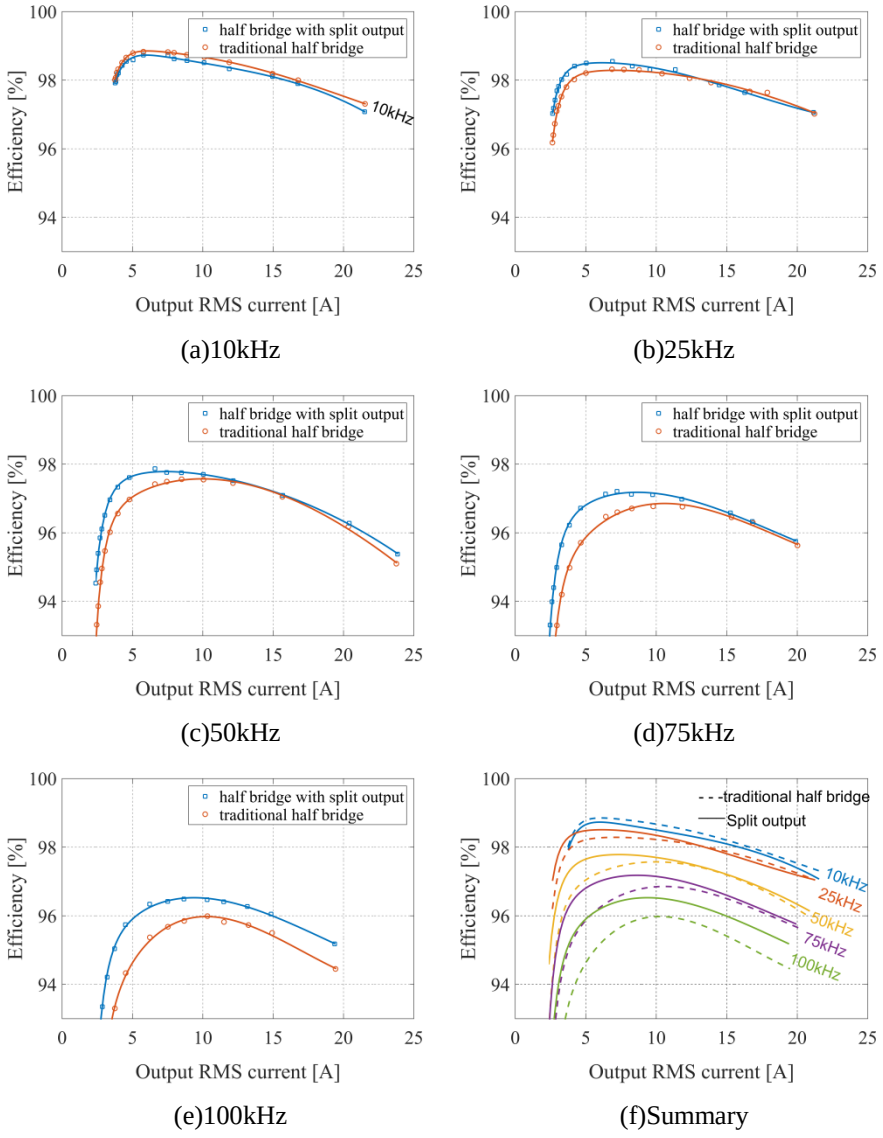


Figure 5.18 Efficiency comparison with difference switching frequencies

5.2 Split output DBC layout

Two half bridge SiC MOSFET power modules are shown in Figure 5.19. One is the Danfoss power module, which is without the external paralleled schottky diodes. The other one is a SiC MOSFET power module from Cree,

which has the external paralleled schottky diodes. The DBC layout of these two power modules are also shown in Figure 5.19. The DBC layouts of these two SiC MOSFET power modules have a common feature: the power current goes through the paralleled dies from one side to the other side. This kind of DBC layout has been analyzed in chapter 4. There are large circuit mismatches and current coupling effect among the paralleled dies, which causes large current imbalance in the switching transient.

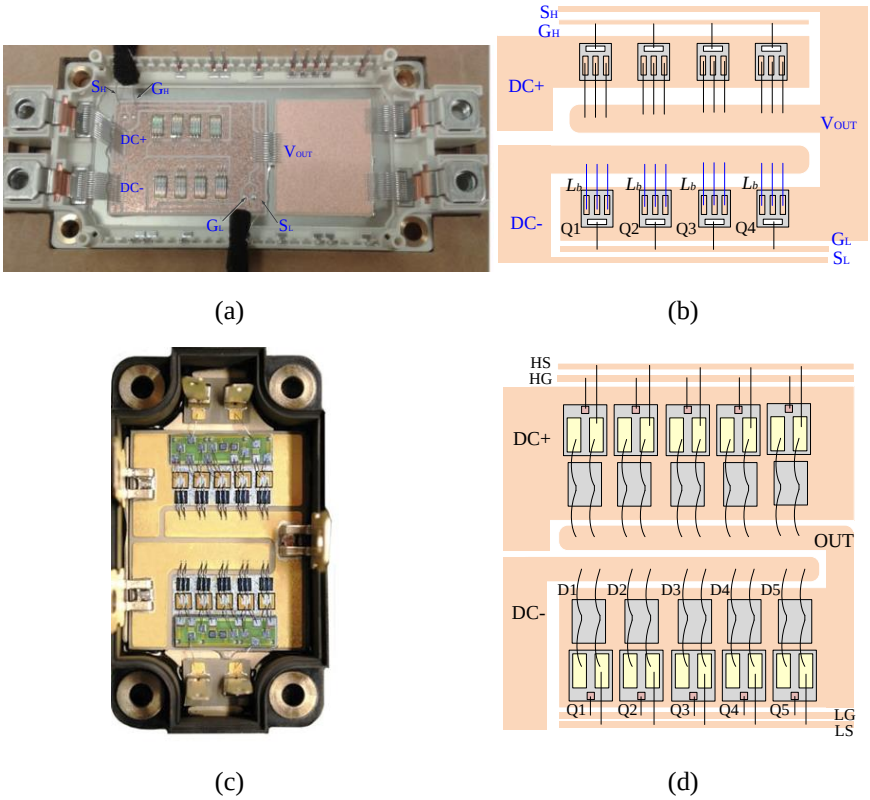
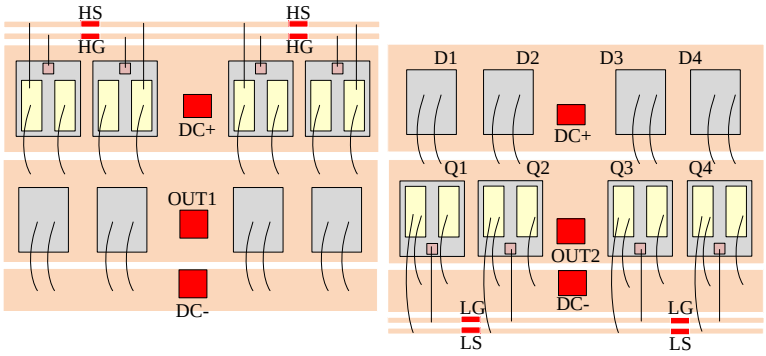


Figure 5.19 Traditional power modules and DBC layouts (a) Danfoss power module (b) DBC layout of Danfoss power module (c) Cree power module (d) DBC layout of Cree power module

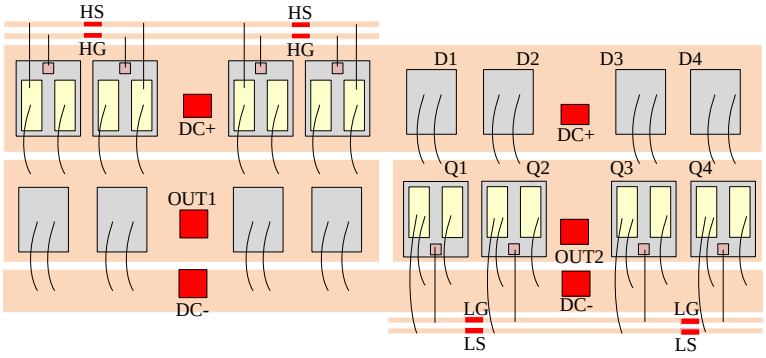
5.2.1 Mathematic analysis of the DBC layout with split output

To reduce the circuit mismatch and mitigate the current imbalance in the power module with paralleled SiC MOSFET dies, a novel DBC layout is proposed, as shown in Figure 5.20. Vertical connectors are located where the

color is red. In the proposed DBC layout, the SiC MOSFETs and the SiC schottky diodes are not paralleled directly. They are organized based on the concept of switching cell[77]. The half bridge power module with this DBC layout works with split outputs. The DBC layout can be split to two separate DBC patterns and encapsulated in two power modules cells, as shown in Figure 5.20(a). The DBC layout can also be packaged in one power module, as shown in Figure 5.20(b). Q_1, Q_2, Q_3 and Q_4 are the four paralleled SiC MOSFET dies while D_1, D_2, D_3 and D_4 are the corresponding diodes which are in the same bridge leg with Q_1-Q_4.



(a)



(b)

Figure 5.20 DBC layout with split output (a) split output DBC layout in two separate power modules (b) split output DBC layout in one power module

With the proposed DBC layout, the paralleled SiC MOSFET dies have a symmetric distribution in a pair of two. For instance, in Figure 5.20(a), there

is no circuit mismatch between Q_1 and Q_4, either between Q_2 and Q_3. The power current in the proposed DBC layout does not go through the DBC trace from one side to the other side, but goes from the two edges of the DBC traces to the center. There are still circuit mismatches between Q_1 and Q_2, also between Q_3 and Q_4. However, the circuit mismatches and the current coupling effect are dramatically reduced compared with the DBC layout in Figure 5.19.

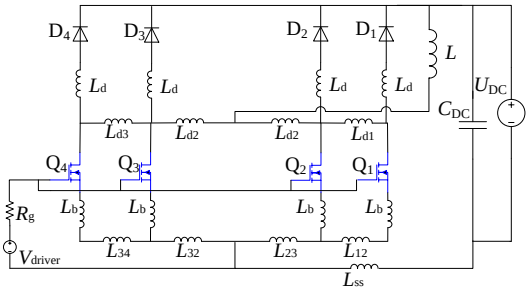


Figure 5.21 Models of the proposed DBC layouts

The circuit models of the traditional DBC layout and the proposed DBC layout are shown in Figure 5.21(a) and Figure 5.21(b), respectively. According to the circuit models, the mathematic analysis of the current imbalance is developed to compare the performance of the DBC layouts. To simplify the mathematic analysis, the auxiliary source bond wires are not included in this model. The difference between with and without the auxiliary source bond wires has been discussed in chapter 4. It is reasonable to simplify the mathematic analysis without the auxiliary source bond wires.

$$i_D = g_{fs}(V_{driver} - i_G R_G - V_{th} - \triangle V_{LS}) \tag{5.1}$$

$$\begin{cases} i_{D1}-i_{D2}=g_{fs}\left[L_b\dfrac{d(i_{D2}-i_{D1})}{dt}+L_{12}\dfrac{d(i_{D2}+i_{D3}+i_{D4})}{dt}\right] \\ i_{D2}-i_{D3}=g_{fs}\left[L_b\dfrac{d(i_{D3}-i_{D2})}{dt}+L_{23}\dfrac{d(i_{D3}+i_{D4})}{dt}\right] \\ i_{D3}-i_{D4}=g_{fs}\left[L_b\dfrac{d(i_{D4}-i_{D3})}{dt}+L_{34}\dfrac{di_{D4}}{dt}\right] \\ i_{D1}-i_{D4}=g_{fs}\left[L_b\dfrac{d(i_{D4}-i_{D1})}{dt}+L_{12}\dfrac{d(i_{D2}+i_{D3}+i_{D4})}{dt}+L_{23}\dfrac{d(i_{D3}+i_{D4})}{dt}+L_{34}\dfrac{di_{D4}}{dt}\right] \end{cases} \tag{5.2}$$

During the switching transient in the saturation region, the drain current of the MOSFET is determined by the gate source voltage, which is presented in (5.1) with the common source stray inductance (L_s) effect. The current imbalance among the paralleled dies in traditional DBC layouts can be calculated as (5.2) while the current imbalance in the proposed DBC layout with split output is given with (5.3) and (5.4).

$$\begin{bmatrix} \triangle V_{LS1} \\ \triangle V_{LS2} \\ \triangle V_{LS3} \\ \triangle V_{LS4} \end{bmatrix} = \begin{bmatrix} L_b+L_{12}+L_{23} & L_{23} & 0 & 0 \\ L_{23} & L_b+L_{23} & 0 & 0 \\ 0 & 0 & L_b+L_{32} & L_{32} \\ 0 & 0 & L_{23} & L_b+L_{32}+L_{34} \end{bmatrix} \begin{bmatrix} i_{D1} \\ i_{D2} \\ i_{D3} \\ i_{D4} \end{bmatrix} \tag{5.3}$$

$$\begin{cases} i_{D2}-i_{D1}=g_{fs}\left[L_b\dfrac{d(i_{D1}-i_{D2})}{dt}+L_{12}\dfrac{di_{D1}}{dt}\right] \\ i_{D2}-i_{D3}=0 \\ i_{D3}-i_{D4}=g_{fs}\left[L_b\dfrac{d(i_{D4}-i_{D3})}{dt}+L_{34}\dfrac{di_{D4}}{dt}\right] \\ i_{D1}-i_{D4}=0 \end{cases} \tag{5.4}$$

With the proposed DBC layout, the transient current imbalance only exists between Q_2 and Q_1 and between Q_3 and Q_4. Moreover, compared (5.2) and (5.4), the current imbalance in the proposed DBC layout is dramatically reduced, especially between Q_1 and Q_4.

As discussed in chapter 4, the auxiliary source bond wires can mitigate the current imbalance among the paralleled dies. In the split output DBC layout, the auxiliary source bond wires have similar effects with that in the

traditional DBC layout. The split output DBC model with the auxiliary source connections are shown in Figure 5.22. In Figure 5.22, it can be observed that the auxiliary source connections are in parallel with the DBC traces between two SiC MOSFETs. For instance, L_{34} is in parallel with L_{bx4}-L_{s34}-L_{bx3} in series. From this point of view, the auxiliary source connections of L_{bx4}-L_{s34}-L_{bx3} can reduce the effective stray inductance between Q_3 and Q_4 and therefore mitigate the current imbalance between Q3 and Q4. With the auxiliary source bonds, the current imbalances are given in (5.5).

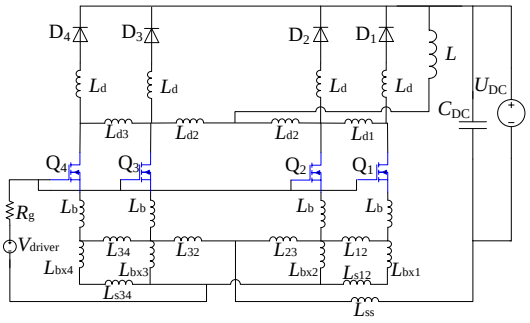
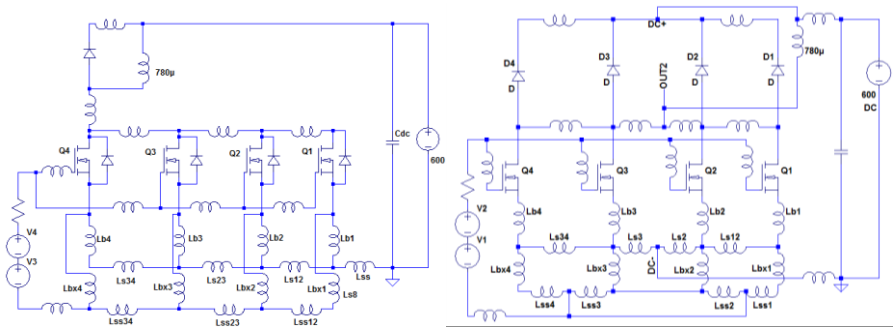


Figure 5.22 Proposed DBC layout model with auxiliary source connections

$$\begin{cases} i_{D2}-i_{D1}=g_{fs}\left[L_b\dfrac{d(i_{D1}-i_{D2})}{dt}+L_{12}\dfrac{L_{bx2}+L_{bx1}+L_{s12}}{L_{bx2}+L_{bx1}+L_{s12}+L_{12}}\dfrac{di_{D1}}{dt}\right] \\ i_{D2}-i_{D3}=0 \\ i_{D3}-i_{D4}=g_{fs}\left[L_b\dfrac{d(i_{D4}-i_{D3})}{dt}+L_{34}\dfrac{L_{bx3}+L_{bx4}+L_{s34}}{L_{bx3}+L_{bx4}+L_{s34}+L_{34}}\dfrac{di_{D4}}{dt}\right] \\ i_{D1}-i_{D4}=0 \end{cases} \tag{5.5}$$

5.2.2. Simulation and experimental study

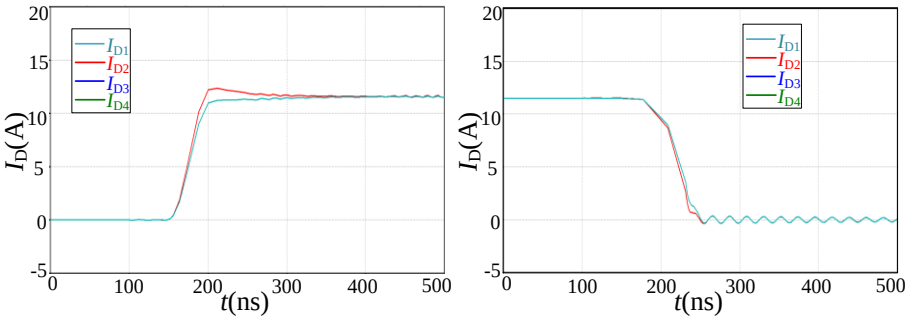
The traditional DBC layout and the split output DBC layout are evaluated with the LTspice simulation. The LTspice simulation circuits of these two DBC layouts are shown in Figure 5.23.



(a) (b)

Figure 5.23 Simulation circuits of the DBC layouts (a) traditional DBC layout (b) proposed DBC layout

The LTspice simulation results are shown in Figure 5.24. With the identical stray inductances of the DBC traces and the bond wires, the current distribution in Figure 5.24 has a smaller current imbalance compared to the current distribution in the simulation results with the traiditional DBC layout. In the simulation results of the proposed DBC layout, the MOSFET Q_1 has the same current of Q_4 while Q_2 has the same current of Q_3. The simulation results validate the mathematic analysis. Besides the mitigation of the current imbalance among the paralleled dies, the die current overshoot in the proposed DBC layout is also reduced due to the more uniform current distribution.



(a) (b)

Figure 5.24 Simulation results with proposed layout (a) turn on (b) turn off

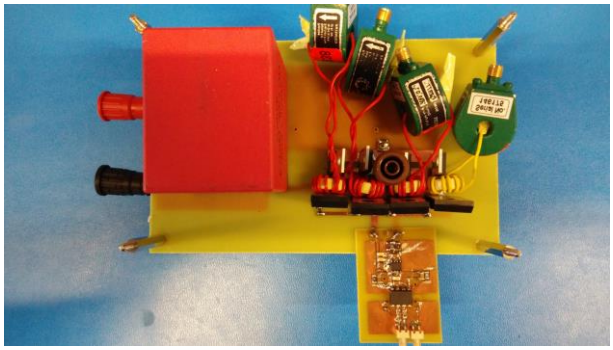


Figure 5.25 Hardware setups

The die current in the power module is hardly measured with an acceptable accuracy at present. Therefore, to experimentally evaluate the current sharing performance with the proposed DBC layout, a PCB circuit with the similar layout of the DBC is developed, as shown in Figure 5.25. The paralleled SiC MOSFETs in the PCB circuit have a common gate driver. The experimental results of the PCB circuit with split output layout are shown in Figure 5.26. This study focuses on transient current performance, which is related to V_{th}. Therefore, the four paralleled SiC MOSFETs are selected with close threshold voltages.

With the comparison between Figure 4.15, Figure 4.25 and Figure 5.26, it is obvious that the paralleled SiC MOSFETs have a smaller transient current imbalance with the proposed DBC layout. The simulation and experimental results verify the mathematic analysis.

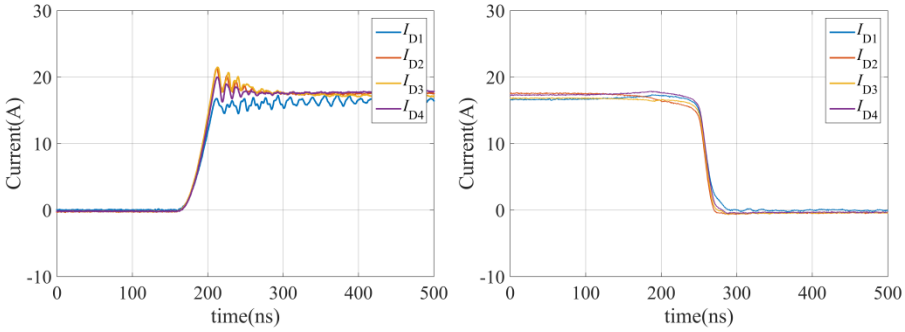


Figure 5.26 Experimental results with the proposed DBC layout

5.3 Conclusion

This chapter makes the analysis of the split output topology with a half bridge circuit. The current commutation process and the efficiency comparison are presented. It shows that the SiC MOSFETs in the half bridge with split output have smaller switching losses compared with that in the traditional half bridge. The efficiency benefits with the split output topology increases with the increase of the switching frequency. The split output is especially suitable for the high switching frequency.

With the understanding of the split output topology, a novel DBC layout for the half bridge power module with paralleled dies is proposed. The proposed DBC layout reduced the current imbalance among the paralleled SiC MOSFET dies by re-organize the circuit stray inductance. With the proposed DBC layout, the current distribution among the paralleled dies in the power module is optimized. Simulation and experimental results validates the mathematic analysis and the effectiveness of proposed the DBC layout.

The proposed DBC layout is not only suitable for paralleling SiC MOSFET in the multichip power module. It can also be used for Si IGBT or MOSFET power modules and SiC JFET power modules. Based on the analysis and the experimental results in chapter 4 and chapter 5, the DBC layout design guidelines for the power modules with paralleled power semiconductors can be concluded. First, more attentions on the stray inductance of the bond wires and the DBC traces are needed. The common source stray inductance in the power module is the most critical stray inductance for the transient switching performance. Second, for the power module with paralleled dies, the mismatch of the common source stray inductance among the paralleled dies largely affects the transient current distribution in the power module. The traditional DBC layout for paralleling dies is not suitable for the fast switching power devices, e.g. SiC MOSFETs and SiC JFETs. Evenly distributing the common source stray inductance for the paralleled dies is a key point to achieve a better current distribution.

6 Conclusion and future work

This chapter presents the summary of the thesis research works and gives some plans about the future work.

6.1 Conclusion

1. The SiC MOSFET switching characterization is experimentally investigated. Guidelines of how to use fast switching power semiconductors are summarized. The fast switching speed of the WBG devices require more attention in terms of packaging technologies and application considerations. The influences of the switching loop stray inductance and the common source stray inductance on the switching performance of SiC MOSFETs are investigated. In the characterization of the SiC MOSFETs, the existed pulse current measurement for the fast switching power semiconductors are experimentally evaluated and compared. A pulse current measurement method with silicon steel current transformer is developed with the merits of high band width, feasible mechanical design and galvanic isolation.

2. The parallel connection of SiC MOSFETs is studied under the influences of device and circuit mismatches. The circuit mismatches influence on the parallel connection of SiC MOSFETs is first investigated and experimentally evaluated. The switching loop stray inductance mismatch causes different drain source voltage overshoots in the paralleled dies. While the common source stray inductance mismatch can lead to transient current imbalance between the paralleled SiC MOSFETs. The transient current imbalance causes extra switching current overshot and switching losses imbalance.

3. With a full understand of the circuit mismatch influence, an investigation of the parallel connection of SiC MOSFETs in the power module is carried out. It is found that there are large circuit mismatches in a traditional DBC layout of the power module with paralleled SiC MOSFET dies. The circuit mismatch in the DBC layout can cause transient current imbalance among the paralleled dies in the power module. Moreover, a current coupling effect in the traditional DBC layout is revealed. The current coupling effect aggravates the transient current imbalance. The mathematic analysis of the DBC layout is presented and the current distribution among the paralleled

dies is experimentally validated. Furthermore, the auxiliary source bond wires in the power module with paralleled dies are studied. The auxiliary source bond wires can reduce the total common source stray inductance for the power module, and it can also mitigate the current imbalance among the paralleled dies. On the other hand, the auxiliary source bond wires are different from the Kelvin-Source connection. The auxiliary source bond wires for the paralleled dies forms extra loops for the power current, which may cause large current pressure on the auxiliary source bond wires and extra oscillations. With the above analysis, the essence of the transient current imbalance among the paralleled dies in the power module is summarized.

4. To mitigate the current imbalance among the paralleled dies, a novel DBC layout is proposed with split output topology. The working mechanism and the benefits of the split output topology are discussed and experimentally demonstrated. The proposed DBC layout is mathematically analyzed and experimentally evaluated. With the comparison to the traditional DBC layout, the proposed DBC layout has a reduced circuit mismatch and current coupling effect. The current distribution among the paralleled dies in the proposed DBC layout is optimized. A new guideline or rule for the DBC layout with paralleled power semiconductor is concluded.

6.2 Future works

The current measurement method with the silicon steel current transformer will be used to investigate the current sharing performance of the paralleled devices in the P3 power module. The P3 power module is made with paralleled half bridges. The difference between paralleled dies and paralleled half bridges will be studied.

The proposed DBC layout with split output topology has been used in 10kV SiC MOSFET power module, which is made in Aalborg University. In the future, there will be more power modules manufactured with paralleled SiC MOSFET dies. In the low voltage range, we will also further investigate the optimization for the parallel connection of SiC MOSFET in the power modules. With the understanding of the circuit mismatch and current coupling effect in traditional the DBC layout, more DBC layouts with

optimized current distributions will be invented and manufactured. These are also going on with other researchers. Anyway, the traditional DBC layout needs to be optimized, especially for the fast switching power semiconductors, e.g. WBG devices.

The thermal performance of the Danfoss power module and the power module with the proposed DBC layout will be investigated. With the thermal investigation, the influences of the transient current imbalance on the thermal performance can be presented.

6.3 Publications

6.3.1 Publication list

1. H. Li, S. Munk-Nielsen, 'Challenges in switching SiC MOSFET without Ringing', *PCIM Europe* 2014, Germany.
2. H. Li, S. Munk-Nielsen, 'Detail study of SiC MOSFET switching characteristics', *PEDG* 2014, Ireland.
3. H. Li, S. Munk-Nielsen, C. Pham, S. Beczkowski, 'Circuit mismatch influence on performance of paralleling silicon carbide MOSFETs', *EPE* 2014, Finland.
4. H. Li, S. Munk-Nielsen, S. Beczkowski, X. Wang, 'SiC MOSFET based split output half bridge inverter: current commutation mechanism and efficiency analysis', *ECCE* 2014, USA.
5. H. Li, S. Munk-Nielsen, X. Wang, R. Maheshwari, S. Beczkowski, C. Uhrenfeldt, Toke Franke, 'Influences of device and circuit mismatches on paralleling silicon carbide MOSFETs', *IEEE Trans. Power Electron.*, 2015.
6. H. Li, S. Beczkowski, S. Munk-Nielsen, K. Lu, Q. Wu, 'Current measurement method for characterization of fast switching power semiconductors with silicon steel current transformer', *APEC* 2015, USA.
7. H. Li, S. Munk-Nielsen, S. Beczkowski, R. Maheshwari, T. Franke, 'Circuit mismatch and current coupling effect on paralleling SiC MOSFETs in multichip power modules', *PCIM Europe* 2015, Germany.

8. S. Beczkowski, H. Li, S. Munk-Nielsen, C. Uhrenfeldt, **‘**10kV SiC MOSFET split output power module**’,** *EPE* 2015, Switzerland.
9. H. Li, S. Munk-Nielsen, S. Beczkowski, X. Wang, ‘A Novel DBC layout for current imbalance mitigation in SiC MOSFET multichip power module’ Submitted to *APEC 2016* and *IEEE Transaction on Power Electronics Letters, 2015*

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